(2)

TECHNICAL MANUAL

FOR

PORTABLE DURESS SENSOR

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Prepared for: U.S. Army Mobility Equipment
Research and Development Command
Procurement & Production Directorate
Fort Belvoir, VA 22060

Prepared by: Sonicraft, Inc.
8859 South Greenwood Avenue
Chicago, IL 60619

DISCLAIMER NOTICE

TECHNICAL MANUAL

FOR

PORTABLE DURESS SENSOR

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TECHNICAL MANUAL

FOR

PORTABLE DURESS SENSOR

SECTION 1

GENERAL INFORMATION

1.1. SCOPE

This technical manual provides detailed information for operation, troubleshooting, repair and maintenance of the Portable Duress Sensor built by Sonicraft, Inc. Also included are parts list information, wiring diagrams, schematic diagrams, installation data and safety information.

1.2. DESCRIPTION AND PURPOSE

1.2.1 GENERAL

The Portable Duress Sensor system consists of one or more hand-held VHF transmitters, a separately enclosed wall or post mounted receiver and a receiver antenna assembly. No accessories are required.

The primary mission of the equipment is to provide an alarm indication when a transmitter is activated. In addition an anti-tamper alarm circuit provides immediate identification if the transmitter case is opened, the receiver enclosure is opened or the receiver antenna or lead-in is disconnected.

1.2.2 TRANSMITTER

The transmitter, Figure 1-1, is a small, lightweight, self-contained unit that can be worn or carried by the user. It is capable of transmitting 256 different code patterns and operates in the VHF range from 265 MHz to 285 MHz. In normal use, the transmitter is activated by two momentary push button switches located on the upper corners of the transmitter. Normal activation requires that both push buttons be pressed simultaneously.

The electrical circuits including the built-in antenna are enclosed in a water tight housing. Operating power is obtained from two 4.5V batteries. The batteries are located under an access cover which when removed trips a tamper switch. This causes the transmitter to transmit an alarm signal to the receiver.

1.2.3 RECEIVER

The receiver, Figure 1-2, is enclosed in a steel housing and has four mounting holes for wall or post mounting.

The unit is a dual conversion superheterodyne receiver with a phase lock loop (PLL) detector for frequency shift keying (FSK) demodulation. The output is decoded into six channels allowing up to six different transmitted codes to be decoded. The channel outputs are combined and applied to a common alarm system. The antenna is attached via an N type coaxial connector at the bottom of the enclosure. Access holes for conduit to bring in external power and for output connections to the alarm circuits are located on top of the enclosure.

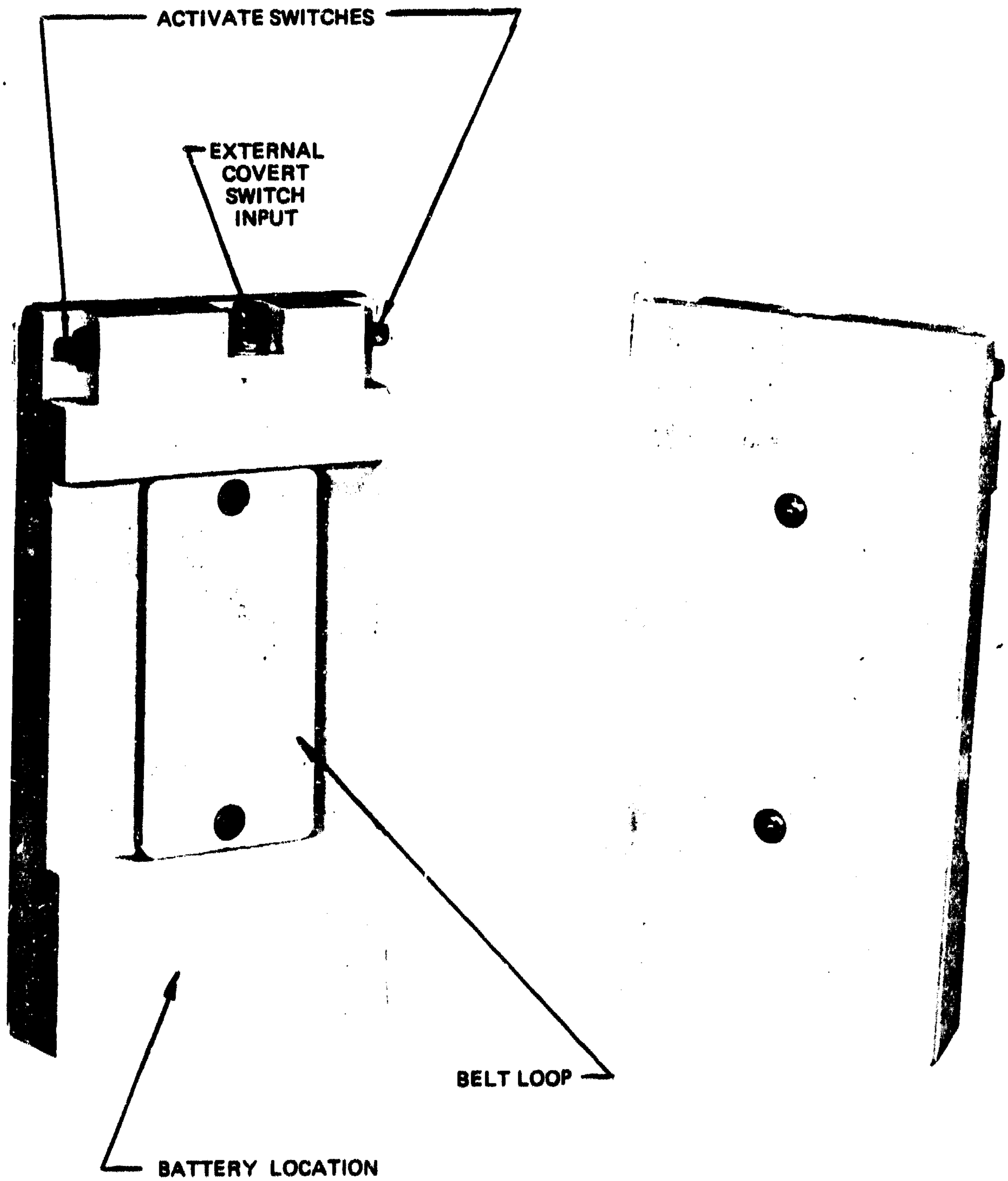


Figure 1-1. TRANSMITTER

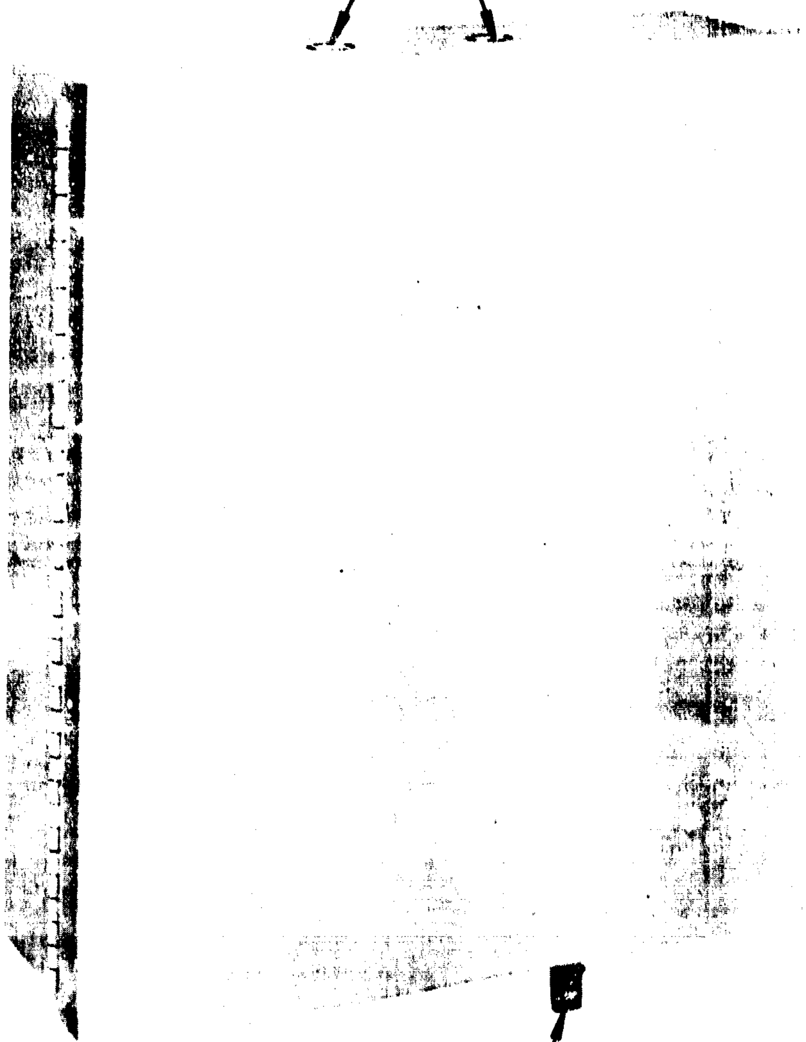


FIGURE 1–2. RECEIVER: NORMAL OPERATING CONFIGURATION

The receiver is designed to be tamper proof. If the antenna is disconnected or the enclosure access door is opened, a tamper alarm is activated.

The receiver, Figure 1-3, contains a printed circuit mother board, six plug-in printed circuit modules, a tamper switch, and a terminal strip for external connections.

The six plug-in modules are:

RF Module

IF Module

Serial/Parallel Converter Module

Decoder Module Channel 1 and 2

Decoder Module Channel 3 and 4

Decoder Module Channel 5 and 6

The decoder modules are interchangeable but must be programmed for the desired channel code.

1.2.4 ANTENNA SYSTEM

The antenna, Figure 1-4, is externally mounted and connected to the receiver via type RG-213 cable with N type connectors. The antenna can be mounted within a maximum 50 foot radius of the receiver.

The antenna is 0.65 wavelength long with a transmission line section providing a dc grounded structure and a 50 ohm rf match to the coaxial cable. The matching components are contained within a circular housing

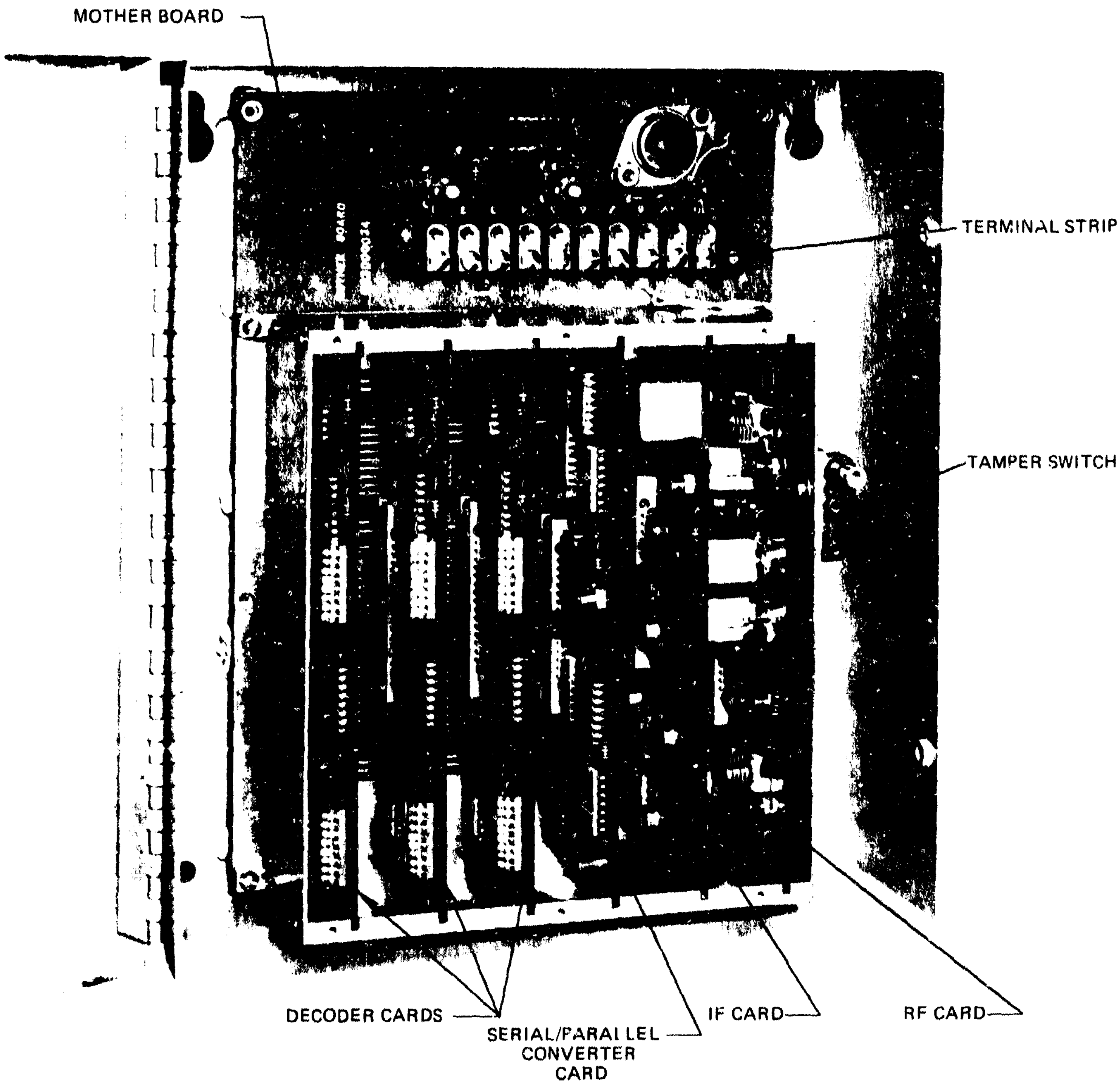


FIGURE 1-3. RECEVER WITH ACCESS COVER OPEN

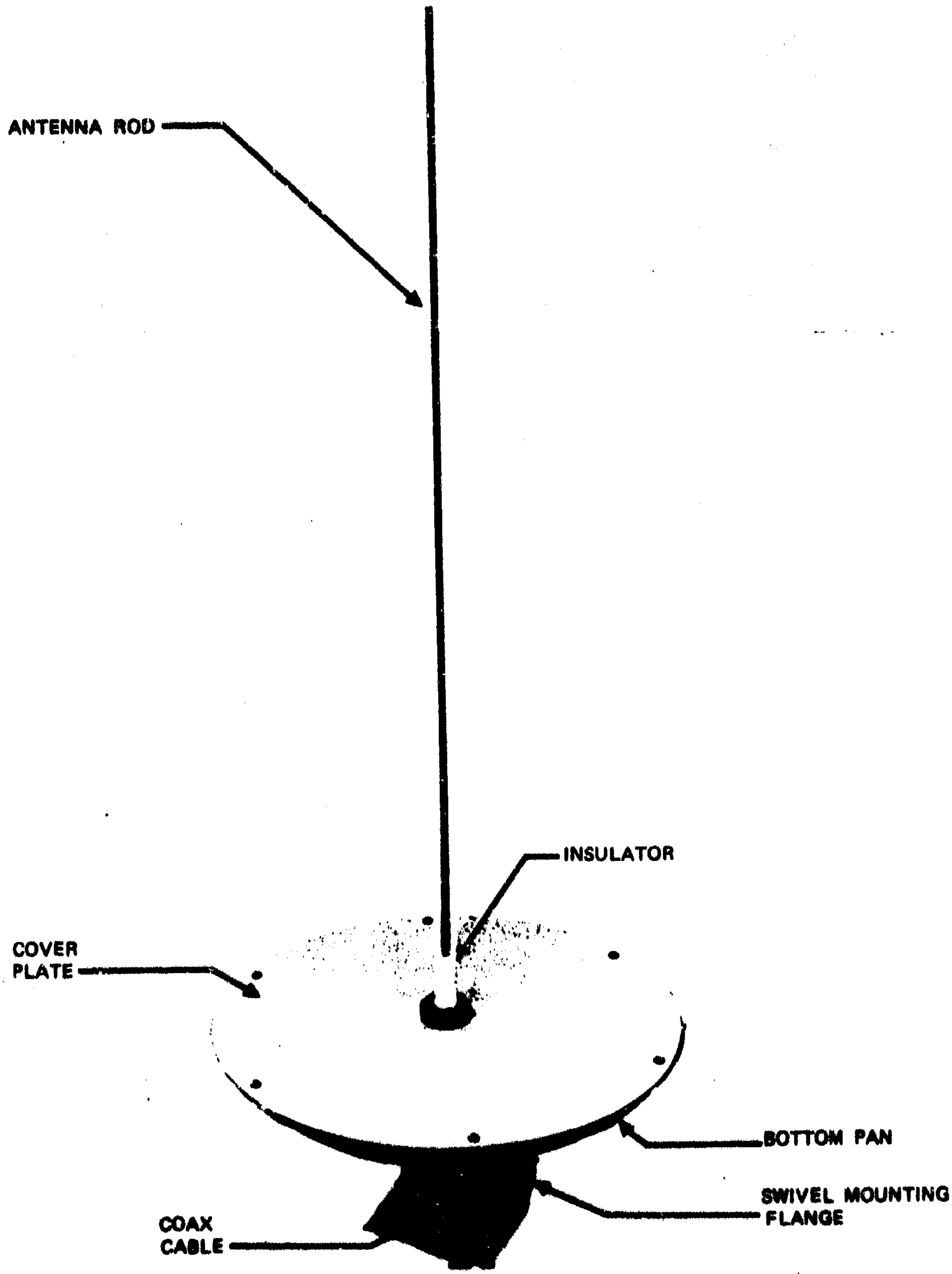


FIGURE 1 – 4. ANTENNA SYSTEM, RECEIVER

that also serves as a ground plane. The dc ground path is used in the anti-tamper circuit. Removal of the antenna or disconnecting the lead-in will result in a tamper alarm being activated.

1.3 SPECIFICATIONS

Specifications for both the transmitter and receiver are provided in Table 1-1.

Table 1-1 Specifications

GENERAL	
Frequency Range	265 to 285 MHz
Temperature Range (Operational)	-40°F to + 150°F
Temperature Range (Non Operational)	-50°F to + 165°F
Humidity	Up to 95% Relative
TRANSMITTER	
Emission	A3, F1
Power Output	20mW
Frequency	Fixed Tuned
Frequency Control	Crystal
Frequency Stability	±0.001%
Modulation	Two Tone FSK, FAM
Number Code Pattern	256
Circuitry	Solid State
Power Source	Two 4.5V Batteries
Activating Device	Pushbutton or External Switch
Transmission Duration	Approx. 52 Seconds
Antenna	Internal
Channels	1

RECEIVER

Tuning	Fixed Tuned
Sensitivity	-106 dBm
External Controls	None
Code Identification Capability	256 Codes
Channels	6
Operating Voltage	20 $\pm$ 1VDC
Maximum Power Input	1.2 Watts
Alarm Output Conditions	100K Ohm Minimum for 1.0 $\pm$ 0.5 Sec. Minimum
No Alarm Output Condition	2K Ohms Maximum

SECTION 2

INSTALLATION

2.1 GENERAL

This section provides detailed information for the receiver and antenna installation. The transmitter is self contained with batteries and antenna and requires no specific installation information.

2.2 SHIPPING INFORMATION

One transmitter, one receiver and one antenna assembly are packaged in a single cardboard carton. Upon receipt, perform a visual check of all components to determine if any damage has occurred in transit.

Retain the shipping carton and packing material for future storage and transport of the equipment.

2.3 POWER REQUIREMENTS

2.3.1 RECEIVER

The receiver is designed to operate from a nominal 20 Vdc source and uses a maximum of 60 mA. Supply voltage can be between 13 Vdc minimum and 30 Vdc maximum. The primary power should be supplied through conduit attached to the receiver enclosure.

2.3.2 TRANSMITTER

The transmitter operates from two internal 4.5 volt batteries.

2.4 INSTALLATION

2.4.1 RECEIVER MOUNTING

Refer to the outline dimensional drawing, Figure 2-1, for spacing of the four mounting holes. Allow sufficient room above the receiver for attaching the power-in and alarm output conduits. Allow sufficient space below unit to connect the RG-213 antenna cable.

Mount the receiver to the mounting surface using 1/4 inch diameter bolts. Bolt heaads should not exceed 1/2 inch in diameter.

NOTE

The receiver housing can be used as a template for locating the mounting holes.

2.4.2 RECEIVER PRIMARY POWER CONNECTION

The primary power should be routed through a 1/2-inch conduit at the top of the receiver enclosure as shown in Figure 2-2.

NOTE

It is recommended that the primary power wires be in a separate conduit from the alarm wires.

Connect the primary power to the terminal strip as follows:

TERMINAL NO.	FUNCTION
7	+ 20 VDC
8	20 VDC RETURN
9	GROUND

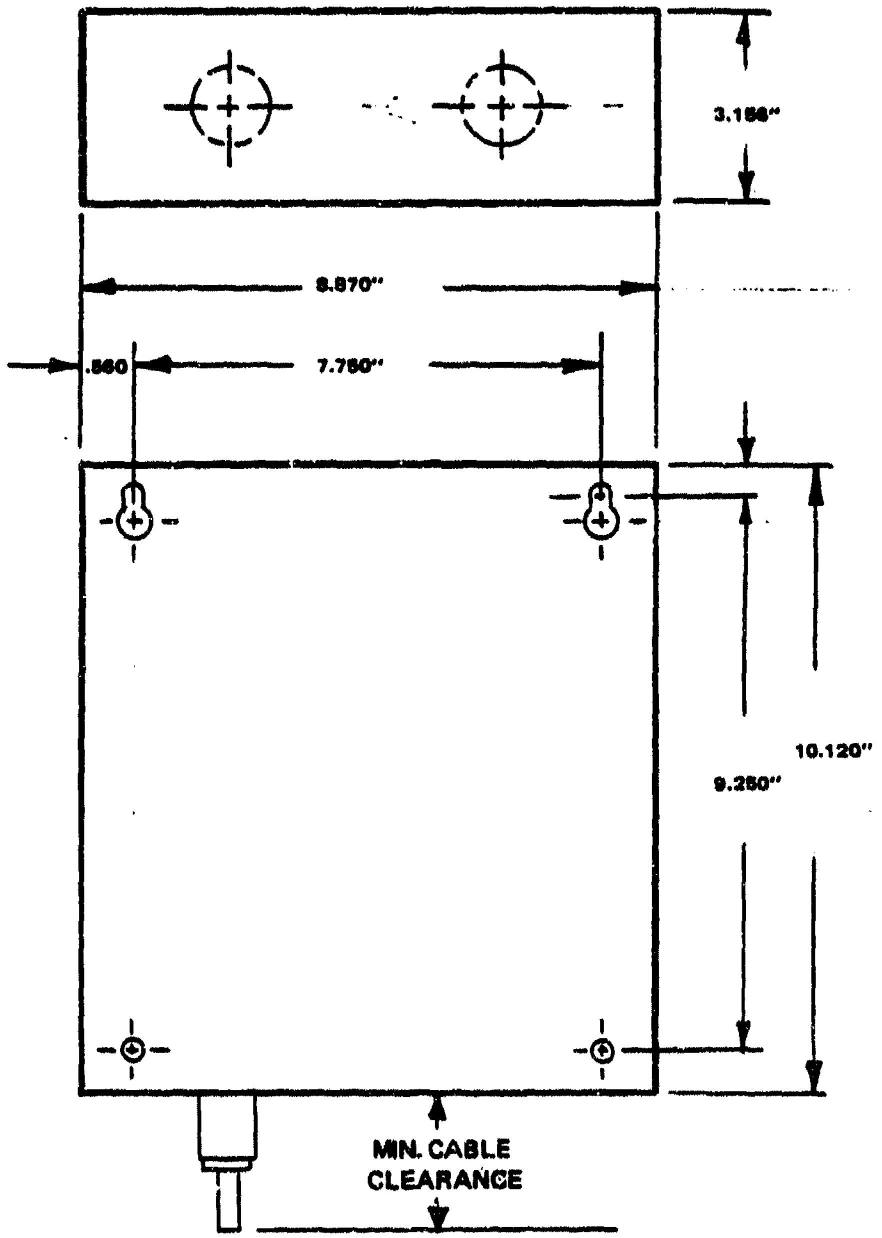
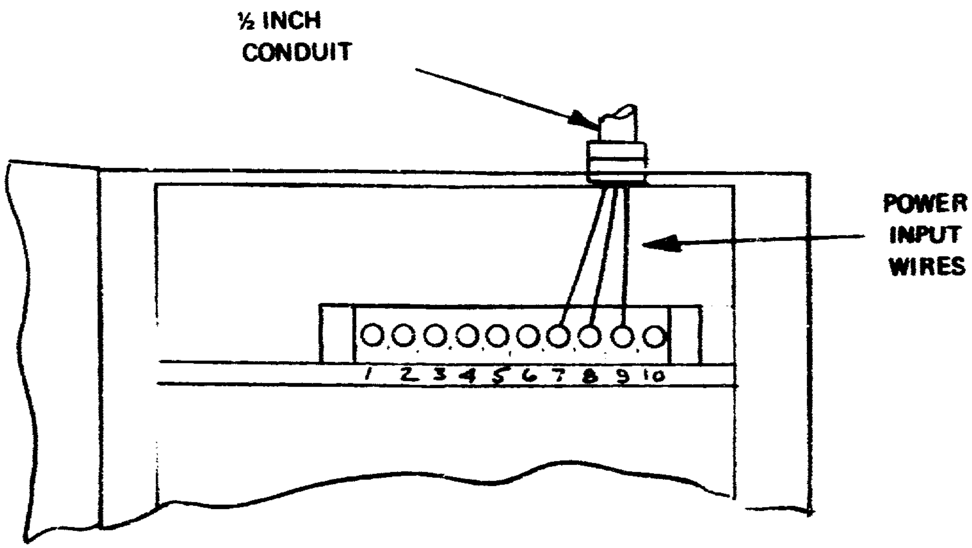


Figure 2-1. Outline Drawing



TERMINAL	FUNCTION
7	+ 20 VDC
8	VDC RETURN
9	GROUND

Figure 2-2. Primary Power Connections

2.4.3 ALARM CONNECTIONS

The alarm wires for both the duress alarm and the tamper alarm should be routed through a 1/2-inch conduit to the terminal strip as shown in Figure 2-3.

NOTE

It is recommended that the alarm output wires be in a separate conduit from the primary power wires.

The receiver is shipped with removable jumpers on the terminal strip between terminals 2 and 3, 3 and 4, and 4 and 5. The use of these jumpers depends on the requirements of the specific installation.

The assignment of terminal strip connections for the alarm outputs are as follows:

TERMINAL NO.	FUNCTION
1	Alarm Output
2	Alarm Output Return
3	Spare
4	Spare
5	Tamper Alarm Return
6	Tamper Alarm

2.4.4 ANTENNA CABLE CONNECTION

The antenna is connected via the supplied coaxial RG-213/U cable through an N-type connector at the bottom of the receiver enclosure.

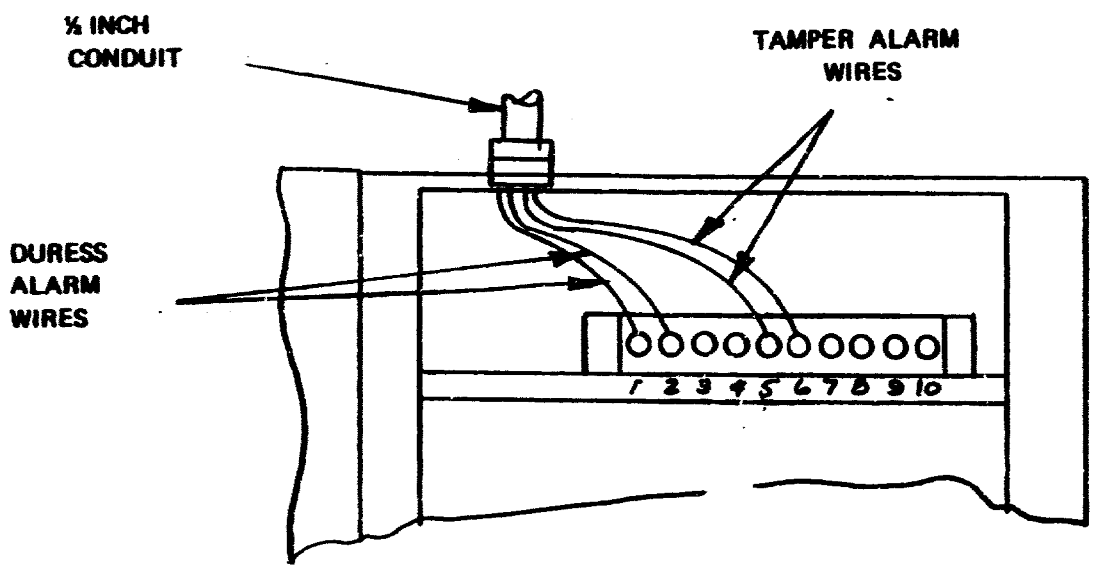


Figure 2-3. Alarm Wiring

2.4.5 ANTENNA INSTALLATION

The antenna, which is illustrated in Figure 2-4, should be located at a height that is clear of surrounding objects to permit maximum signal reception from most distant transmitter. Select a location within the coaxial cable length from the receiver mounting.

2.4.6 TRANSMITTER INSTALLATION

The transmitter, which is illustrated in Figure 2-5, is a portable self contained unit with internal antenna and batteries. The unit can be hand carried, inserted in a pocket, or attached by a belt inserted through the slot in the case. The unit should be worn for easy access to the push-button switches used to activate it.

2.4.7 TRANSMITTER BATTERY INSTALLATION

CAUTION

Opening of the transmitter case for battery replacement will initiate an alarm.

Two 4.5 Volt alkaline batteries are provided for the transmitter power source. To remove old batteries and install new ones proceed as follows:

a. Loosen the two screws, (see Figure 2-6), located on the front of the unit.

NOTE

The printed circuit board will remain attached to the front cover with connecting wires to switches and batteries attached within the case.

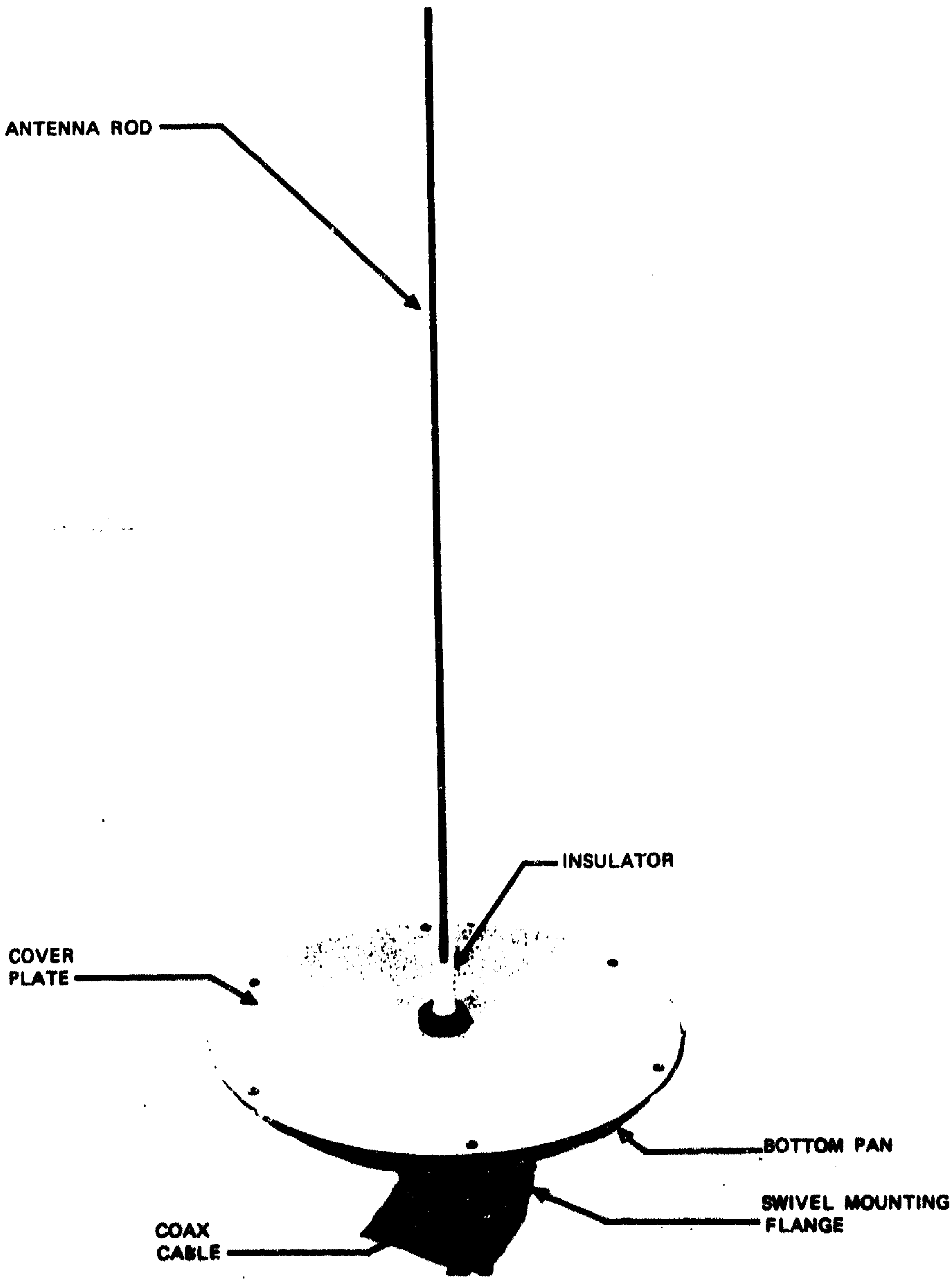


FIGURE 2 – 4. ANTENNA SYSTEM, RECEIVER

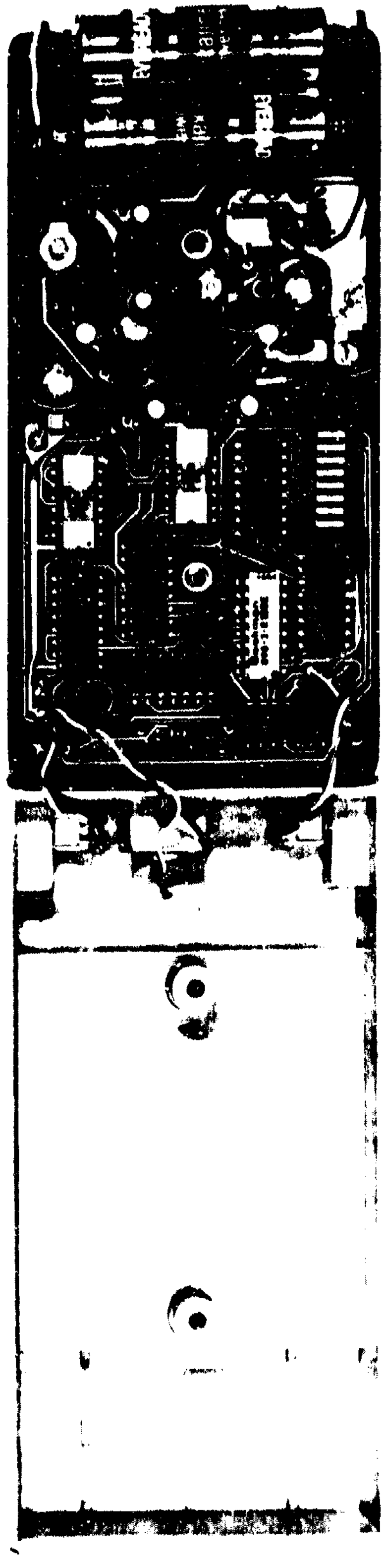
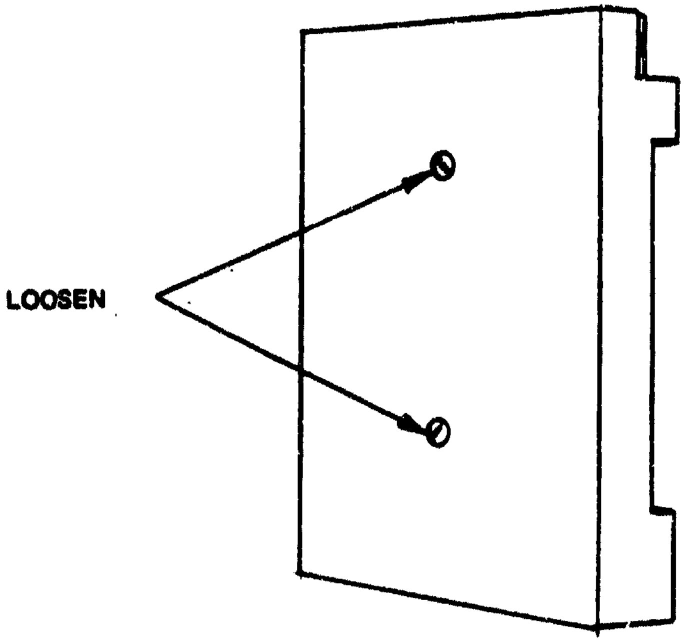


FIGURE 2-5. TRANSMITTER



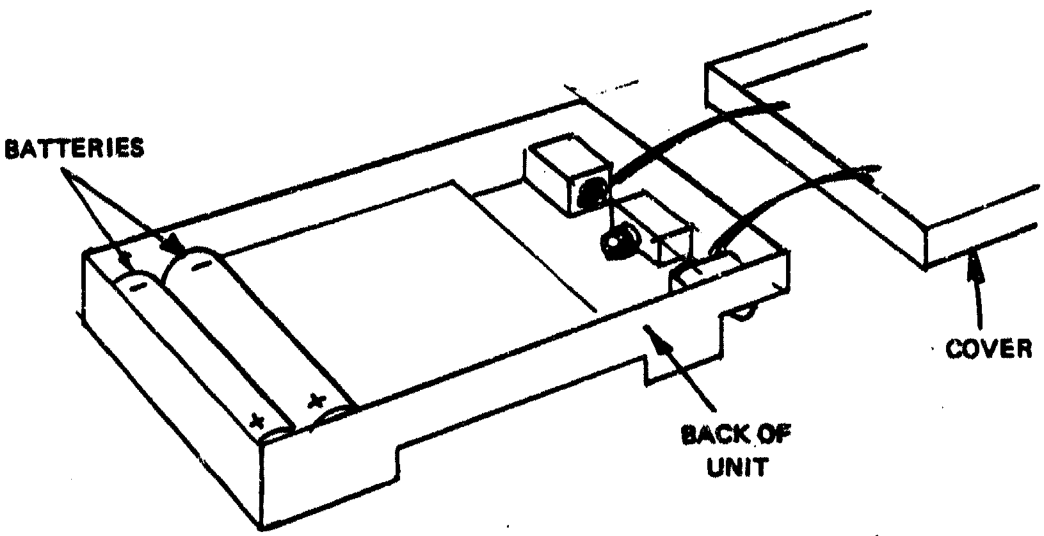


Figure 2-6. Battery Installation

b. Lift back housing off, being careful not to break connecting wires and lay sections next to each other.

c. Lift out battery hold-down.

CAUTION

Observe battery polarity

d. Insert new batteries into clips being sure to observe correct polarity.

e. Place hold-down on top of batteries.

f. Attach cover and housing sections by tightening the two screws firmly. The batteries are held in place by the housing.

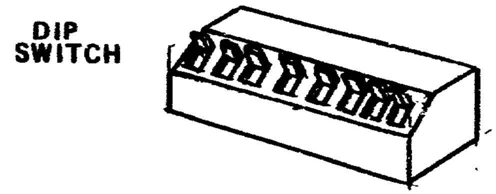
2.5 SETTING CODES

2.5.1 GENERAL

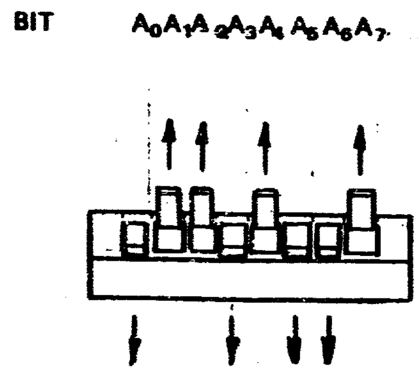
Both the transmitter unit(s) and the receiver unit must be properly set with the desired code(s) in order to initiate a proper alarm. The transmitter has a DIP switch assembly consisting of eight switches which are set for the desired code pattern. The receiver has six channels each of which has a DIP switch assembly with eight switches. Each receiver switch assembly can be set for a different channel code to match appropriate transmitter codes.

The receiver channel code must match the transmitter code to initiate a valid alarm.

The code switch assembly appears as shown in Figure 2-7A. Each switch assembly contains eight switches which can be placed in the open or closed



A. Typical Switch



B. Typical Code Setup

SC110

Figure 2-7. Dip Switch Code Positions

position. The open position represents a binary 1 and the closed position represents a binary 0. The Code bits are designated A0, A1, A2, A3, A4, A5, A6, A7. In any code sequence the first bit from the left is A0 and the bit at the extreme right is A7. For example, if the selected eight bit code is 01101001, the switches would be positioned as shown in Figure 2-7B.

2.5.2 SETTING TRANSMITTER CODE SWITCHES

Determine the required code and proceed as follows to set up the code pattern.

CAUTION

Opening of the transmitter housing will initiate an alarm.

a. Loosen the screws, (See Figure 2-6), located on the front of the unit.

NOTE

The printed circuit board will remain attached to the front cover with connecting wires to switches and batteries attached within the case.

b. Lift front cover off being careful not to break connecting wires and lay sections next to each other.

c. Locate the DIP switch on the printed circuit card. The end of the switch closest to the batteries is bit A0. (Switch No. 1)

d. Set the switches for the required code using illustration Figure 2-7 for reference.

e. Reassemble the unit and tighten screws firmly.

2.5.3 SETTING RECEIVER CODE SWITCHES

The receiver contains 6 channel outputs. Each channel can be set for a different code. Determine which channel(s) are to be set and the required code. The location of the DIP switch assembly for each channel is shown in Figure 2-8. Proceed as follows to set up the code patterns.

CAUTION

Opening the receiver access door of an operating receiver system will activate the tamper alarm.

a. Open receiver access door.

b. Disable tamper switch by pulling out on plunger.

c. Remove printed circuit board hold-down plate by removing the three screws at the top and three screws at the bottom. This will expose the three decoder boards which contain the DIP switches.

d. Determine the codes to be set with the proper channels.

e. Set desired codes with code switches. The end of the switch assembly marked "A0" in Figure 2-8 is the position for code bit "A0" which is marked "1" on the switch assembly.

f. Reinstall printed circuit board hold-down plate and screws.

g. Enable tamper switch by pushing in on plunger.

h. Close access door and secure with the two screws.

2.6 SYSTEM CHECKOUT

The system should be checked out prior to connecting the alarm outputs to the user's control unit. This checkout procedure assumes that primary power has been connnected, that the receiver antenna is connected, that

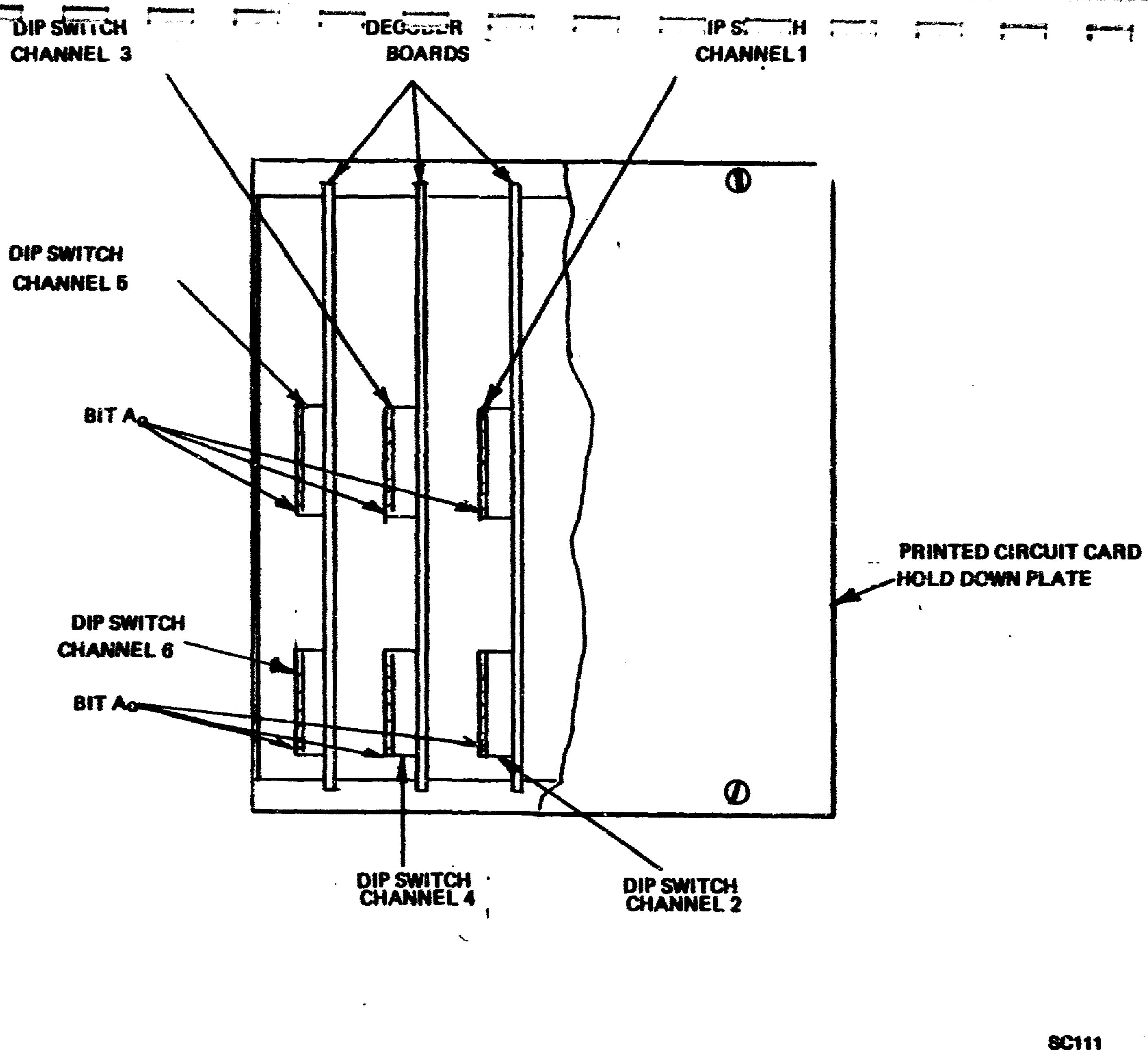


Figure 2-8. Receiver Dip Switch Identification

the transmitter batteries are installed and that codes have been properly set up on the DIP switch assemblies in both the transmitter and the receiver Check out the system as follows using Figure 2-9 as a setup reference.

a. Open receiver access door.

b. Pull out on tamper switch plunger.

c. Check that primary power is properly connected.

d. Check that antenna is properly connected.

e. Check that jumpers are removed between terminals 2-3, 3-4 and 4-5.

f. Connect the two 100K 1/4 Watt resistors to terminals 1 and 6 as shown.

g. Connect other end of resistors together and connect to +10 Vdc source such as U2-3 on printed circuit mother board.

h. Check receiver tamper alarms as follows:

   1. Connect vertical input of oscilloscope to TB1-6 and connect oscilloscope ground to TB1-5. Set oscilloscope for dc measurements. Oscilloscope should indicate about 0.5 Vdc.

   2. Unlatch the tamper switch. Oscilloscope should indicate 10 Vdc.

   3. Relatch tamper switch and lock to service position Oscilloscope should indicate about 0.5 Vdc.

   4. Disconnect antenna cable from receiver. Oscilloscope should indicate 10 Vdc.

   5. Reconnect antenna cable to receiver. Oscilloscope should indicate about 0.5 Vdc.

i. Check transmitter for normal operation.

   1. Disconnect oscilloscope vertical input from TB1-6 and connect to TB1-1. Disconnect oscilloscope ground from TB1-5 and connect to TB1-2.

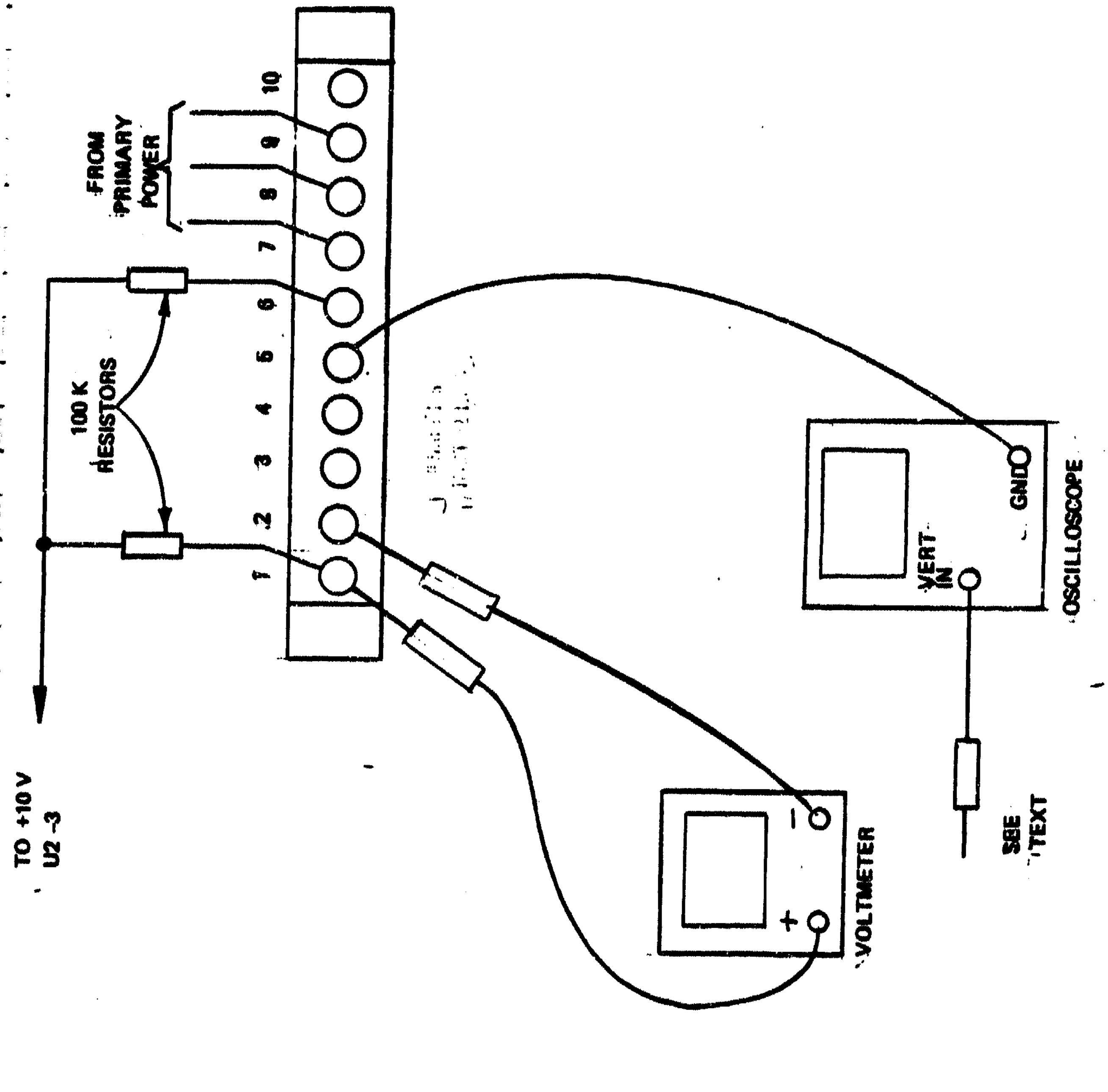


Figure 2-9. Checkout Test Setup

2. Oscilloscope should show about 0.5 Vdc.

3. Momentarily depress the two push-buttons on the sides of the transmitter simultaneously. Transmitter should transmit for about 52 seconds. During this period, DC level on oscilloscope should alternate between 0.5 Vdc and 10 Vdc. The 0.5 Vdc level, however, should be observed for most of the transmission interval and up to 10 seconds after the transmitter tunes out.

NOTE

The actual duration of the 0.5 Vdc level is not important as long as the duration exceeds 1 second.

j. Check transmitter tamper circuit.

1. Check that oscilloscope is indicating about 0.5 Vdc on terminal TB1-1.

2. Loosen the two screws holding the transmitter housing together. When two sections of housing are separated, the transmitter should automatically transmit. The oscilloscope should show a DC level alternating between 10 Vdc and 0.5 Vdc.

NOTE

The actual number of oscillations is not important as long as some occur.

3. Reassemble Transmitter.

k. Repeat steps i and j for each transmitter in the system. If a failure is indicated, first check the codes set into the transmitter

and be sure a matching code exists in one of the receiver channels.

SECTION 3

OPERATION

3.1. GENERAL

During use, the Portable Duress Sensor system should be in a standby condition ready for immediate activation. The receiver is on with primary power applied. The transmitter unit has operating voltage applied at all times when a battery is installed.

3.2 RECEIVER OPERATING PROCEDURE

The receiver is in a standby operational mode at all times and does not require any action from an operator.

3.3 TRANSMITTER OPERATING PROCEDURE

The transmitter is normally carried in the hand or may be attached to the wearing apparel of the operator with the belt loop on the back of the case. The operator should keep the transmitter in a position that allows immediate access to the two push-buttons on the sides of the case.

Initiate a transmission by momentarily and simultaneously pushing in on both push-buttons as shown in Figure 3-1.

Operation of the transmitter can also be initiated by connecting an external normally closed switch at the connector located on top of the transmitter. To initiate a transmission this switch must remain open for a period of 4.5 $\pm$ 0.5 seconds minimum.

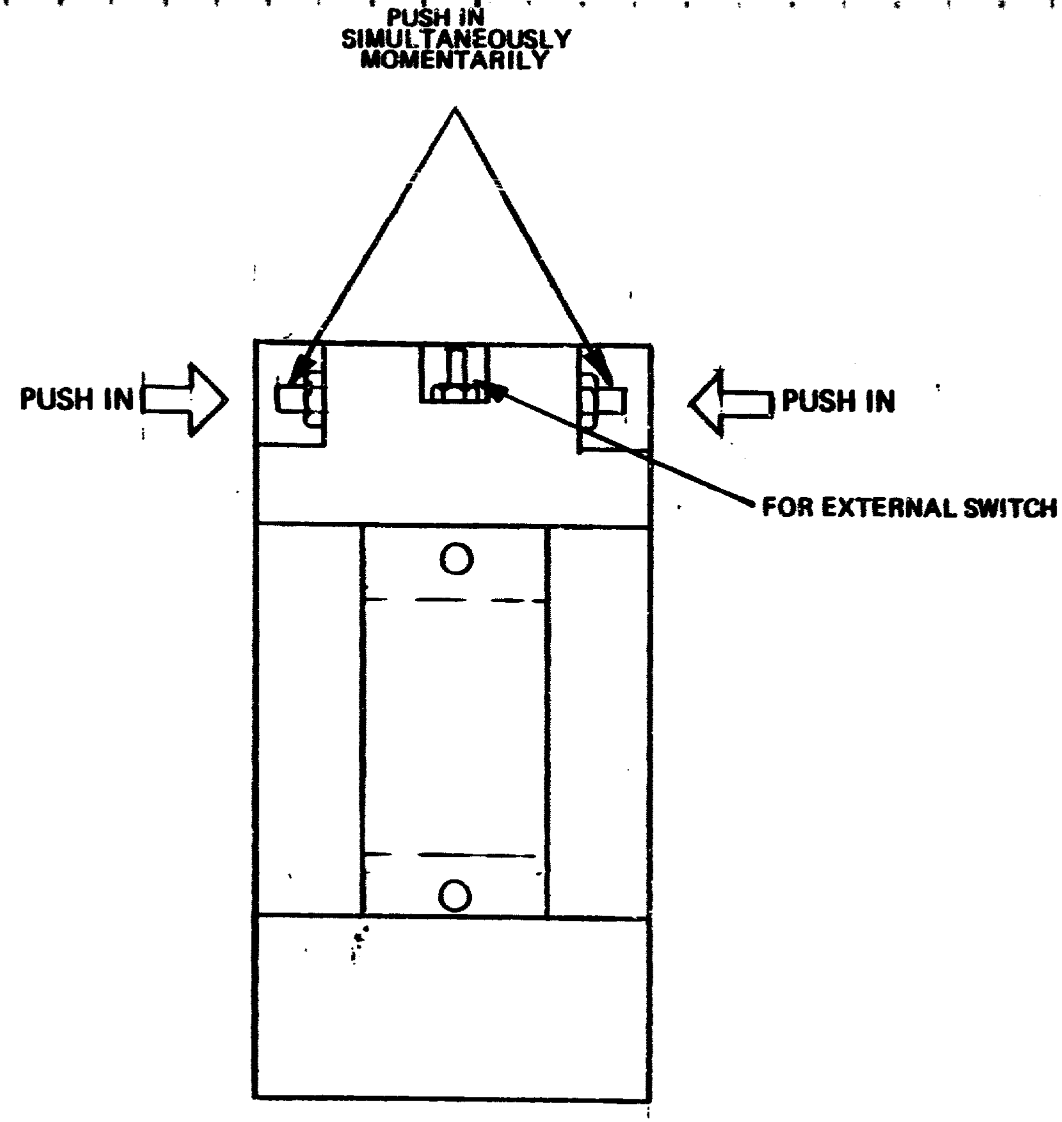


Figure 3-1. Transmitter Operating Controls

SECTION 4

THEORY OF OPERATION

4.1 INTRODUCTION

The theory of system operation is discussed first in terms of a simplified block diagram. The transmitter and receiver theory is then expanded to provide detailed information to aid in troubleshooting the system.

4.2 SYSTEM BLOCK DIAGRAM

The system is designed to provide an alarm output whenever the operator activates the transmitter or when the receiver or transmitter is tampered with. Identification of a specific transmitter is possible because each transmitter incorporates an 8-bit code selection circuit. Thus, there are $2^8=256$ different transmission codes which can be set in the transmitter. The receiver includes decoders (6 maximum). Each decoder can be set to match any one of the 256 transmitter codes.

Operation is normally initiated when the operator simultaneously and momentarily depresses the two switches S1 and S2 (Figure 4-1). This turns on a system time control which activates the clock circuit and starts the generation of a transmission sequence. The system "on-time" control enables the rf oscillator which operates between 66.25 MHz and 71.25 MHz. The oscillator output is applied to two doubler stages in series providing four times multiplication of the base frequency. The doublers also receive a modulation signal from the encoder board. This modulation signal is generated by the FSK generator and is either an 8 kHz signal when a "1" bit is to be transmitted or 10 kHz signal when a

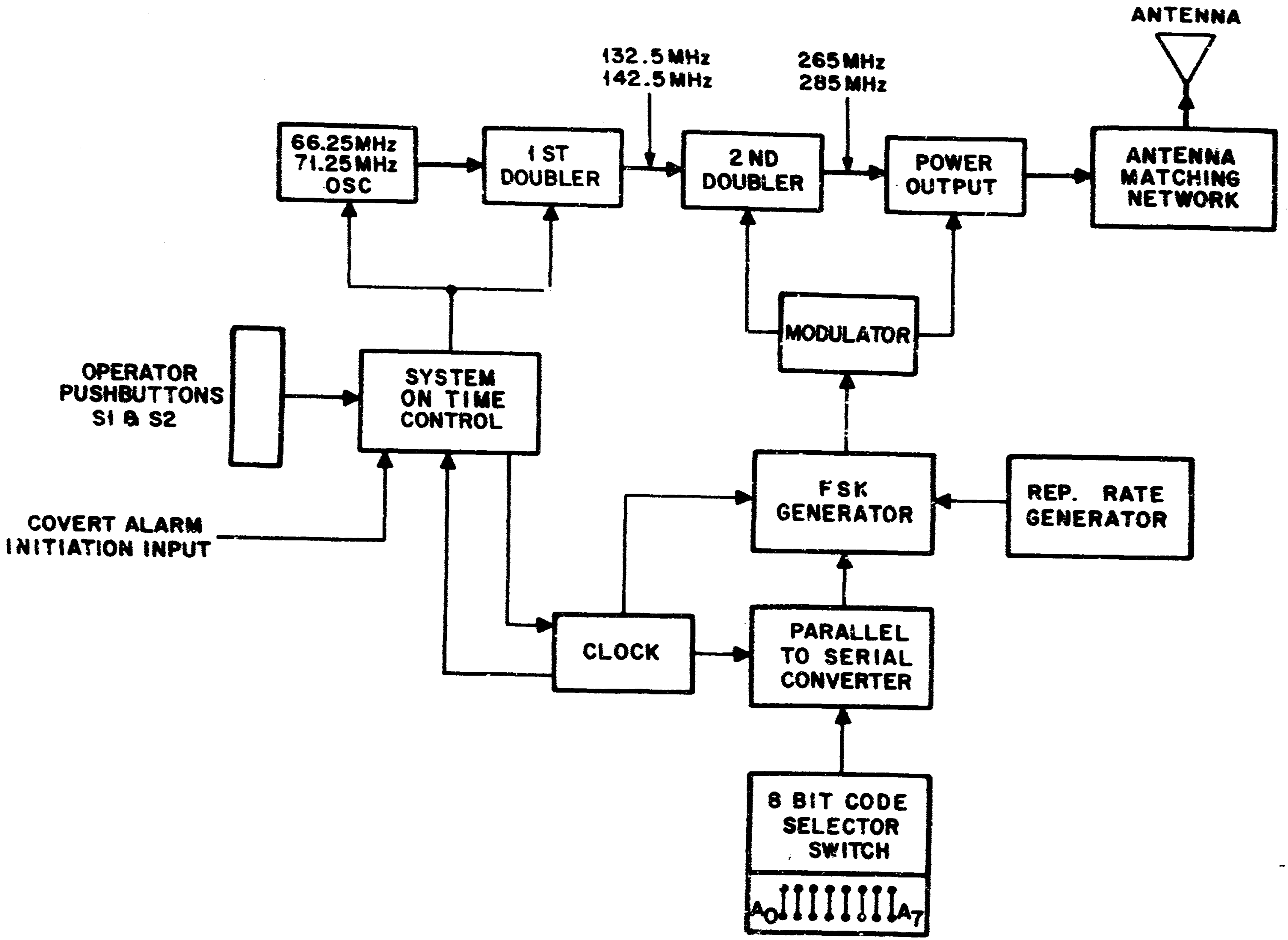


Figure 4-1. Transmitter System Block Diagram

"0" bit is to be transmitted. The encoding signal is constructed as shown in Figure 4-2. Note that there are five "1"s transmitted followed by one "0" at the beginning of each sequence. This is followed by the eight code pulses formed by the setting of the eight bit code selector switch assembly. These pulses may be "1"s or "0"s depending on the position of the bit switches. This is followed by two more "1"s. This pulse sequence is developed in the parallel to serial converter and is about 25.6 milliseconds in length. The transmitter rep rate generator causes the transmitter to repeat this sequence every 400 milliseconds for a period of about 52 seconds or 128 transmissions. The five pulses transmitted at the beginning and two pulses transmitted at the end of each transmission form the bracket pulses for the 8-bit code sequence. The modulated signal at the output of the second doubler is a 275 MHz signal amplitudemodulated with 8 kHZ for each transmitted "1" and 10 kHz for each transmitted "0". This signal is amplified in a class "C" rf power amplifier stage and radiated by the antenna. The transmitted signal will also be initiated if the tamper switch is activated. This will occur whenever the case is opened. The transmission can also be initiated by an external, normally closed switch, connected via cable to the transmitter.

The transmitted signal is picked up by the receiver (Figure 4-3) antenna and amplified in an rf amplifier circuit. The rf amplifier contains two down converters and a band pass filter. The first converter provides a 60 MHz i-f and the second provides the 10.7 MHz i-f output which is applied to the i-f amplifier. The i-f amplifier circuit output is applied to a square law AM detector. The detector output is applied to signal

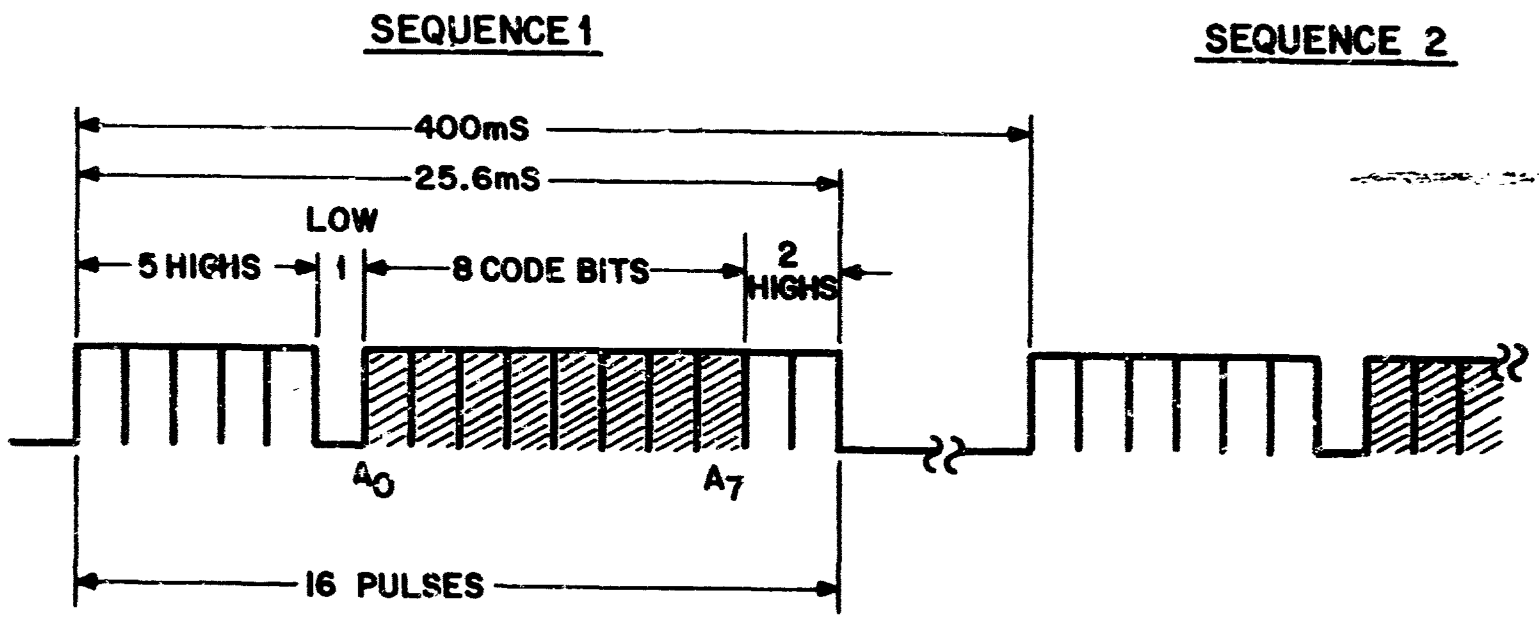


Figure 4-2. Transmitter Pulse Train

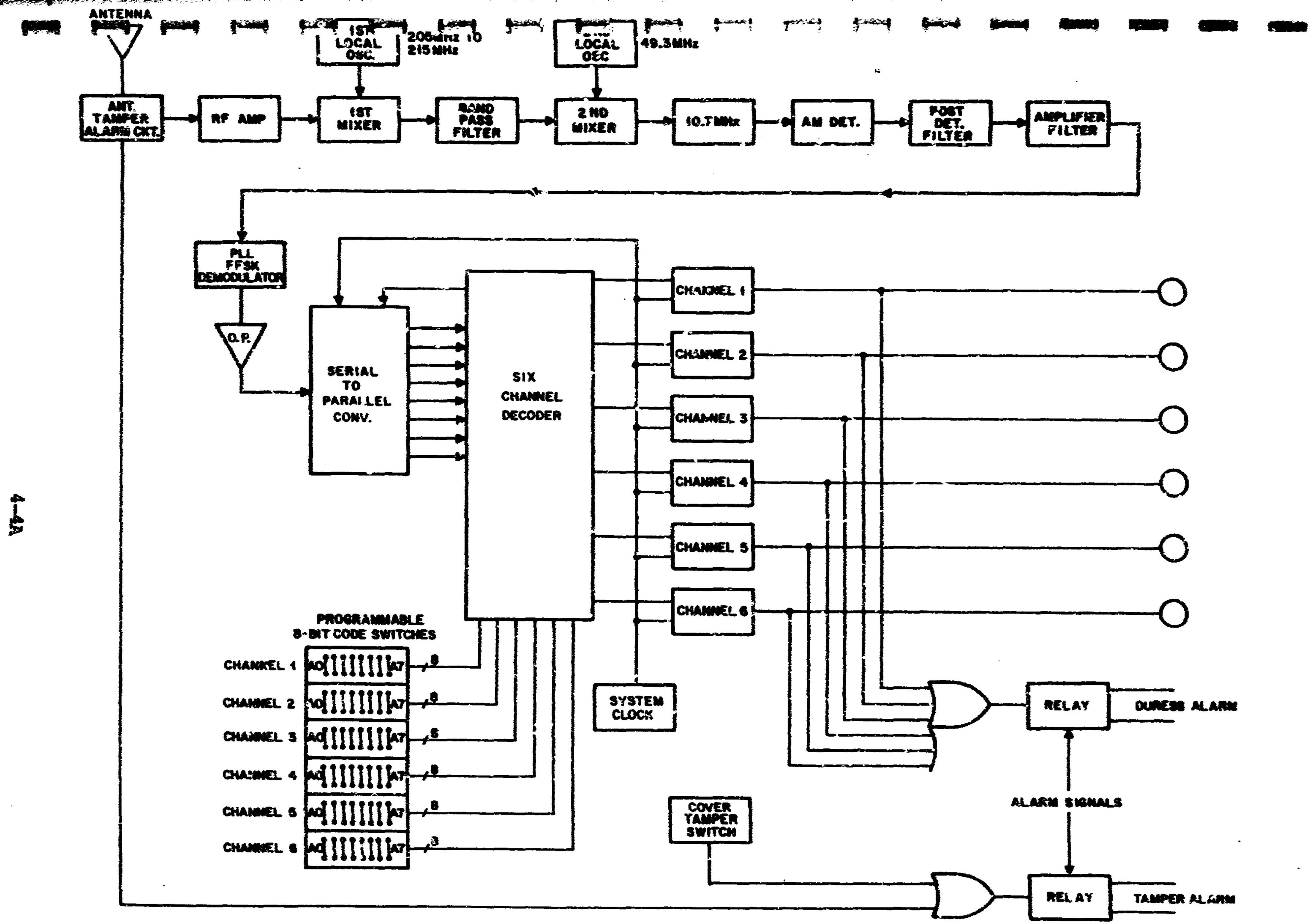


Figure 4-3. Receiver Block Diagram

limiters, then to a phase locked loop for FSK demodulation. The serial output code is converted to a parallel output format in the serial/parallel converter. The parallel output code is applied to comparators in the decoder board where the parallel input code is compared to preset codes on the 8-bit code switches. If an exact match of "1"s and "0"s occurs, the channel provides an output to the alarm circuit.

The receiver also contains a tamper alarm circuit. This circuit is activiated if the antenna or antenna cable is disconnected or if the access door to the receiver is opened. The tamper alarm and duress alarm output are fed to an external control panel. An "alarm" condition is indicated by an output impedance of 100K ohms or more and a "no alarm" condition by an output impedance of 2K ohms or less.

4.3 DETAILED CIRCUIT ANALYSIS

4.3.1 TRANSMITTER

4.3.1.1 GENERAL

The transmitter consists of two main sections. These are the digital encoding circuits and the rf circuits. Refer to the schematic diagrams at the end of this section.

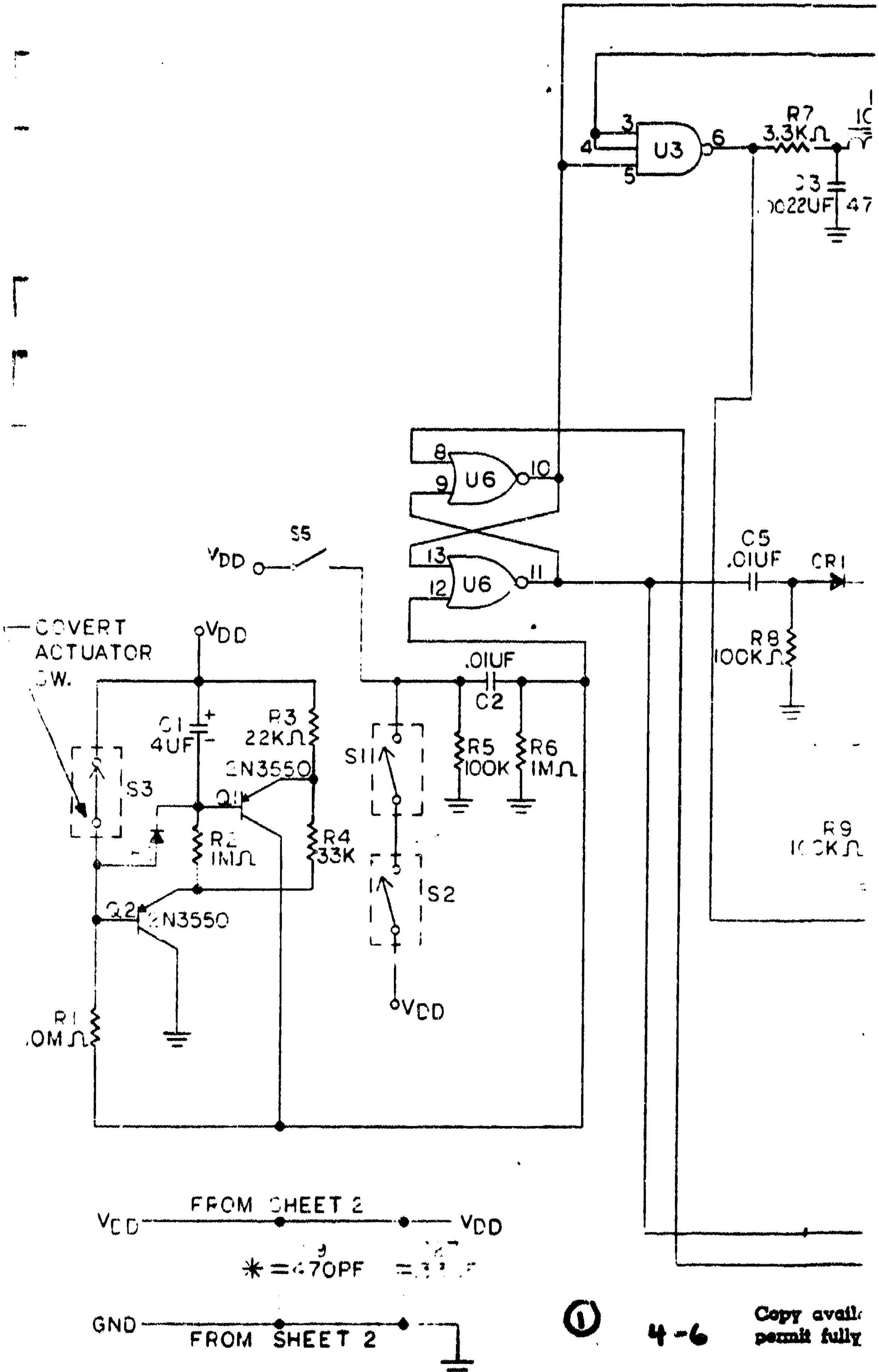
4.3.1.2 DIGITAL ENCODING CIRCUIT

The transmitter digital encoding circuit is shown in Figure 4-4. A transmission can be initiated in the following three ways:

a. By simultaneously depressing the operator switches S1 and S2.

b. By opening the transmitter case causing tamper switch S3 to close.

c. By Opening the covert actuator switch.



U3
R7
3.3KΩ
C3
.0022UF
47
U6
S5
VDD
C5
.01UF
CR1
R8
100KΩ
COVERT
ACTUATOR
SW.
VDD
.01UF
C2
C1
4UF
R3
22KΩ
2N3550
S1
R5
100K
R6
1MΩ
S3
Q1
R2
1MΩ
R4
33K
R9
S2
Q2
2N3550
R1
VDD
FROM SHEET 2
VDD
VDD
* = 470PF
GND
FROM SHEET 2

①

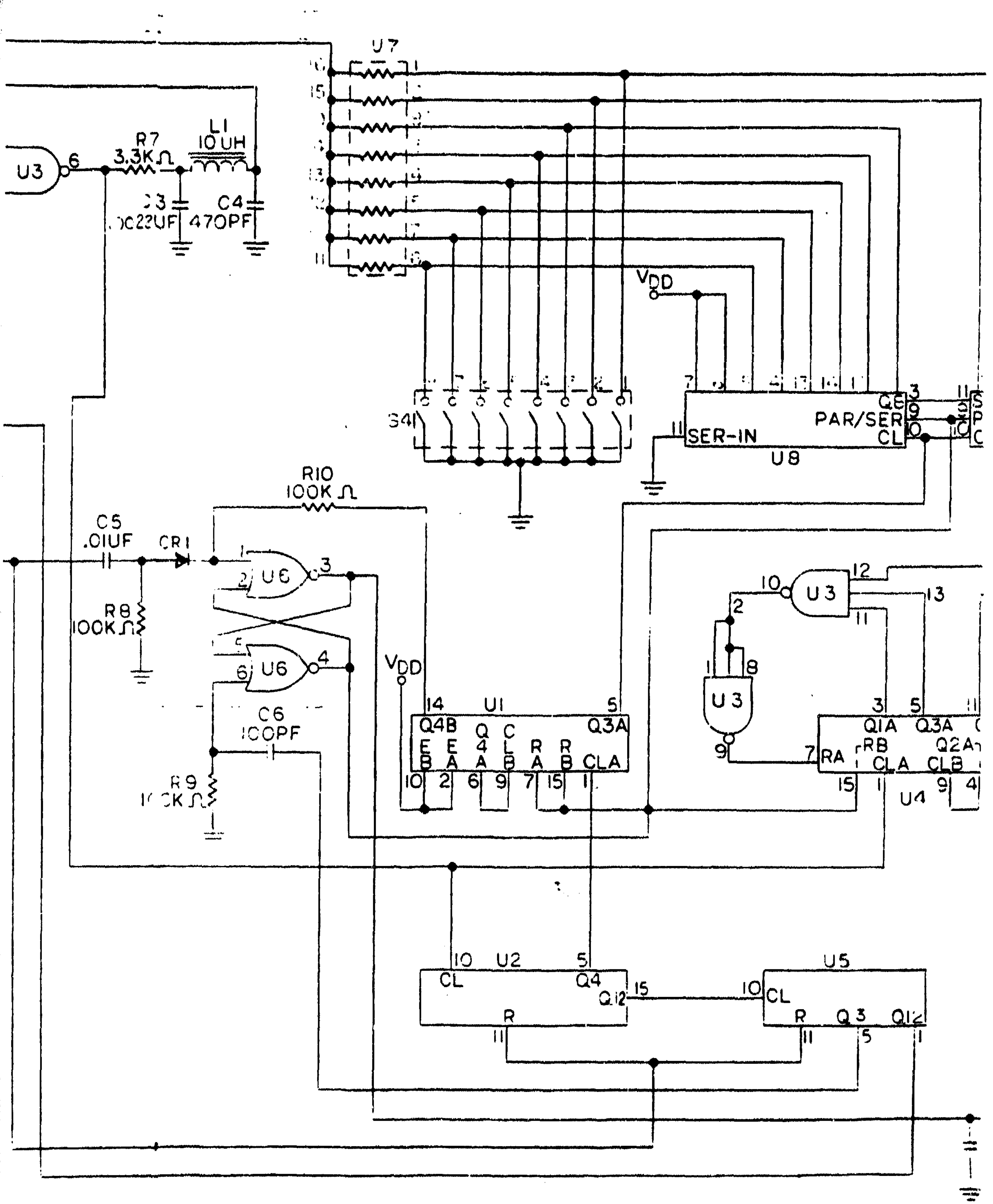
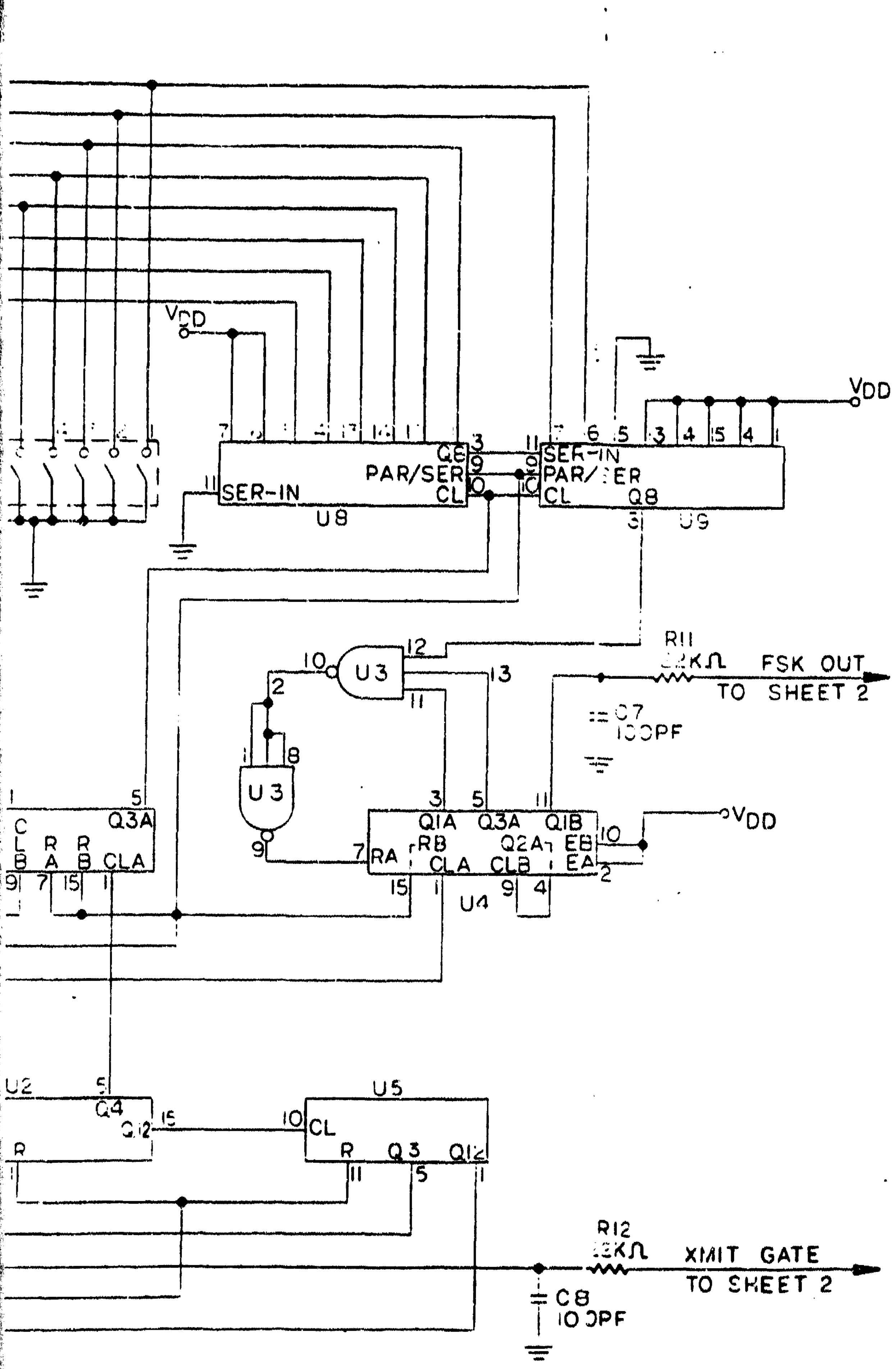

U7
U3
R7
3.3KΩ
L1
10UH
C3
C4
470PF
V_DD
S4
SER-IN
PAR/SER
QE
CL
U8
R10
100KΩ
C5
.01UF
CR1
R8
100KΩ
U6
C6
100PF
R9
U1
Q4B
Q3A
EB
EA
Q4A
CLB
RA
RB
CLA
U4
Q1A
Q2A
U2
Q4
Q12
R
U5
Q3

Figure 4



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4-6

Figure 4-4. Transmitter Digital Encoding Circuit Schematic

3

In conditions a or b the switch closing applies voltage VDD to the differentiator C2--R6 producing a positive pulse output. The positive pulse applied to U6-12 sets the ON time latch U8. In condition c, opening the covert switch removes the short across C1. As C1 charges toward voltage VDD, Q1 is turned on. This also provides pulse output to U6-12 turning on the On-time latch.

NOTE

If the external covert switch is not used, a shorting connector must be used in its place to prevent transmissions.

When the on time latch is set, the high at U6-11 resets and turns on counters U2 and U5. The 80kHz clock output is applied to U2-10. The (U2-5) output is 5 kHz and is applied to counter U1 which is initially disabled, thus does not count. The output at U2-12 (approx 20 Hz) is applied to counter U5. The Q3 output at U5-6 provides a 2.44 Hz square wave (400 millisecond). The initial output is applied to the rep rate latch at U6-6 turning the latch on. The high (a transmit gate) at U6-3 is applied to the rf oscillator gating the oscillator on. At the same time the low at U6-4 resets and turns on counter U1 and enables the parallel/serial shift register U8 and U9. The 5kHz input at U5-1 is counted down to 625 Hz at U5-5 and is applied to the shift registers U8-10 and U9-10 clock inputs. The 625 Hz output at U1-5 clocks the shift register generating a 16 pulse train at the Q8 output (U9-3). The pulse sequence consists of five "1s" (U9-7, 6, 5, 4, 13) one "0" (U9-14), code pulses A0 through A7 (U9-15, 1 and U8-7, 6, 5, 4, 3, 14) followed by two

"1s" (U8-15, 1). The code pulses A0 through A7 depend on the position of the switch section S4A through S4F. A closed switch provides a high (1) output and an open switch provides a low (0) output. The FSK generator U4 counts down the 80 kHz input by a factor of 5 or 4 producing a 20kHz output when U3-12 is a high (divide by 4) and a 16 kHz (divide by 5) output when U3-12 is low. Thus the "1s" and "0s" are converted into 16 kHz or 20 kHz signals. The output of the FSK generator is further divided down by a factor of two to obtain 8 kHz and 10 kHz FSK frequencies.

Since 16 pulses are generated in sequence and the shift register is shifted at a 625 Hz rate, a sequence is completed in 16 X 1/625=25.6 ms. At the end of the 16th pulse U1-14 swings high. This is applied to the rep rate generator at U6-1 resetting the generator. The low at U6-3 turns off the rf oscillator and the high at U6-4 inhibits counter U1, FSK generator U4 and resets the shift register. Note that counter U2 is still counting. At the end of 400 milliseconds, the high at U4-6 again sets the rep rate latch at U6-6 and starts a new transmission cycle. This continues with a 25.6 millisecond pulse output followed by about 375 milliseconds of off time for 52 seconds (128 transmissions). At this time counter output Q12 at U5-1 produces a high output. This is applied as a reset to the on time latch at U6-8, resetting the latch. The low at U6-10 turns off the 80 kHz clocks at U3-5 and the high at U6-11 resets counters U2 and U5. The high at U6-11 is differentiated by C5-R8 and the positive pulse output is coupled through steering diode CR1 to reset the rep rate latch insuring that the Xmit gate output at U6-3 is a low level gating off the rf oscillator.

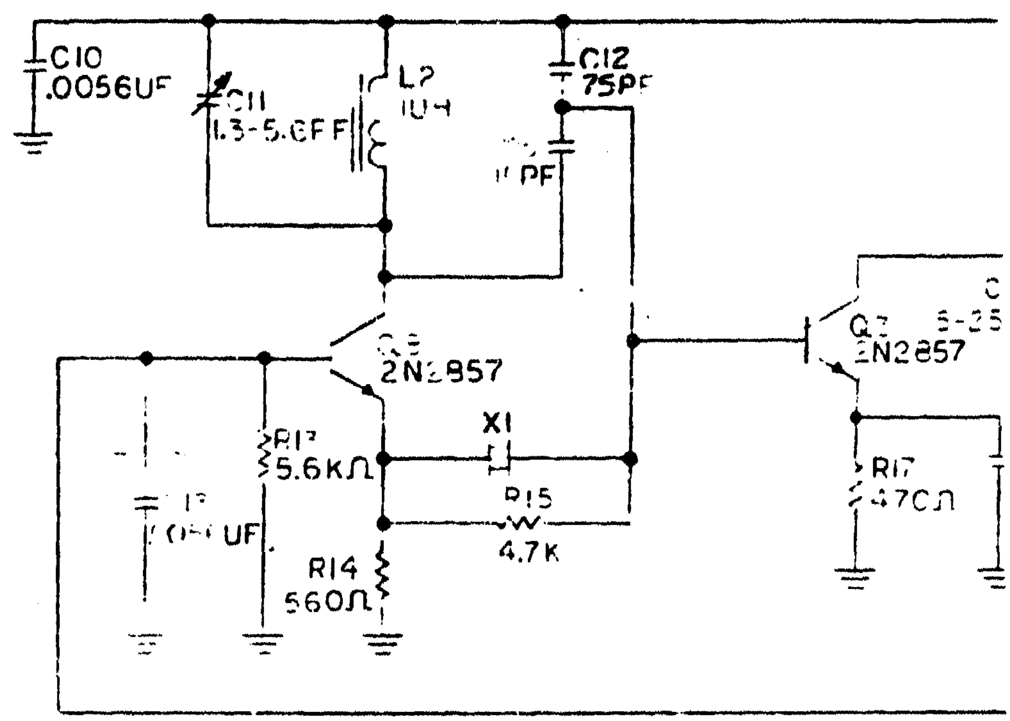
4.3.1.3 RF CIRCUITS

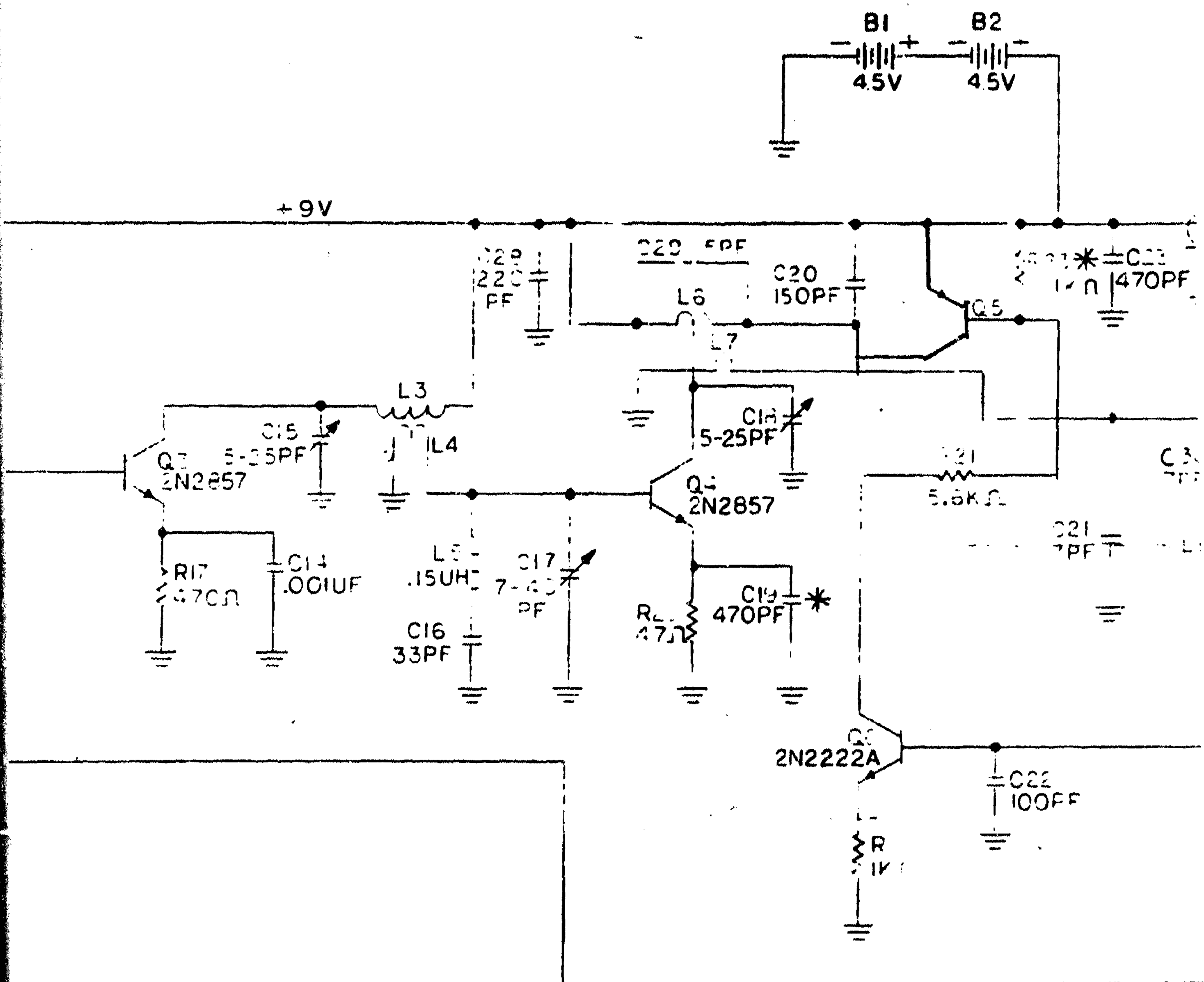
The rf oscillator Figure 4-4 is enabled by a high voltage (Xmit Gate) applied to the base of Q8. The crystal is selected to provide an output frequency between 66.25 and 71.25 MHz with a stability of ± .001% over the temperature range of - 40°F to + 150°F. The low level rf output signal is coupled to doubler Q3 where the frequency is doubled and then applied to a second doubler Q4. The 8 kHZ or 10 kHZ FSK generator output is applied through modulator transistors Q6 and Q5 to the doublers turning the stages on and off at the FSK signal rate. providing pulse amplitude modulation of the rf signal. The modulated output signal is applied to a class "C" rf power amplifier Q7. At proper output level, Q7 draws about 20 ma collector current. The power amplifier output is fed to the antenna system. The antenna system consists of a dipole fed through an antenna matching circuit. The two sections of the dipole, consisting of the transmitter half and the digital half of the printed circuit board, are rf isolated but at the same time provide dc continuity. The matching circuit consists of a tapped transmission line section which allows the antenna to be properly driven by the rf output stage.

4.3.2 RECEIVER CIRCUITS

4.3.2.1 GENERAL

The receiver consists of an rf module, an if module, a serial to parallel converter module, three identical decoder modules and a mother board which contains interconnection facilities, a voltage regulator, and alarm gates.


C10
.0056UF
C11
L2
1UH
C12
75PF
2N2857
5.6KΩ
X1
R15
4.7K
R14
560Ω
2N2857
R17



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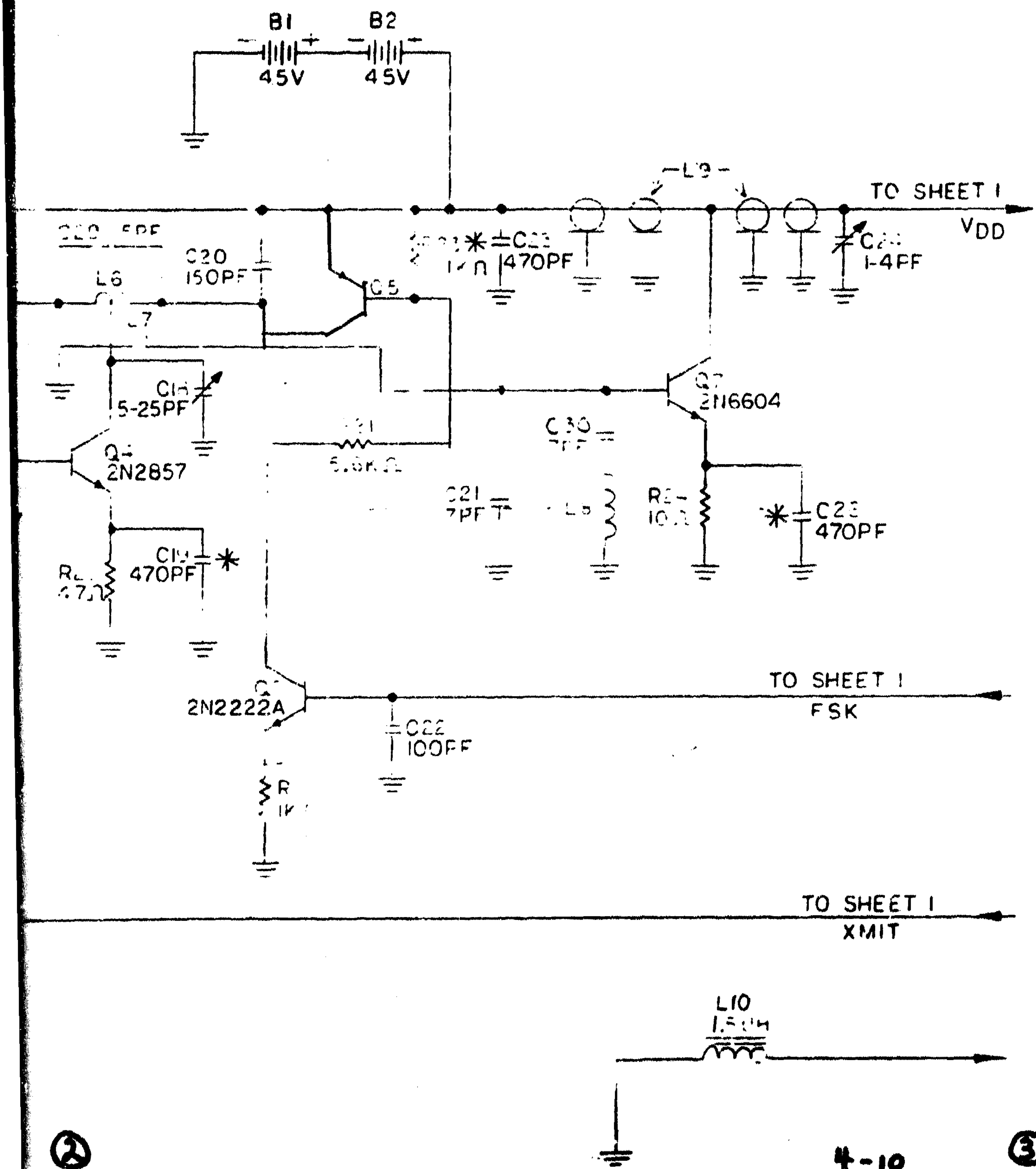
4-10

2



②

③

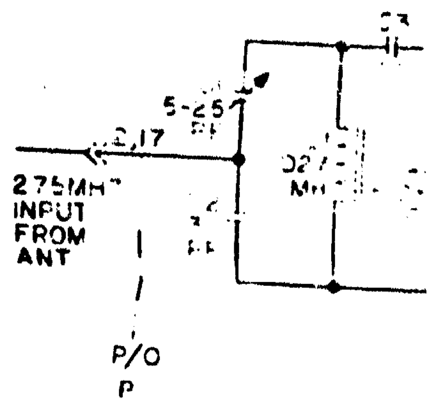
Figure 4-5. Transmitter RF Schematic

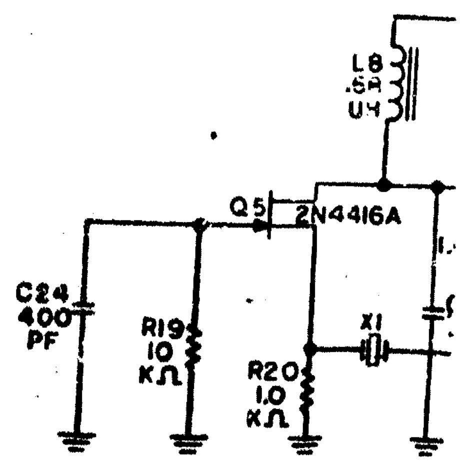
4.3.2.2 RF CIRCUIT BOARD

The AM rf signal picked up by the receiver antenna is applied to a low noise FET rf stage Q1, Figure 4-6. The amplified rf output is applied to mixer Q2 where it is mixed with the 3rd harmonic of the 1st local oscillator Q6. The oscillator base frequency is crystal controlled and selected between 68.33 MHz and 75 MHz. The 3rd harmonic output of 205 to 225 MHz is selected to be 60 MHz below the desired incoming signal. The local oscillator output is mixed at mixer Q2 with the incoming frequency to obtain the 60 MHz first IF. The 60 MHz is amplified by Q3 and applied to gate 1 of mixer Q4. The 49.3 MHz local oscillator signal from Q7 produces an output IF of 10.7 MHz. The 10.7 MHz signal is then applied to the 10.7 MHz. IF amplifier board.

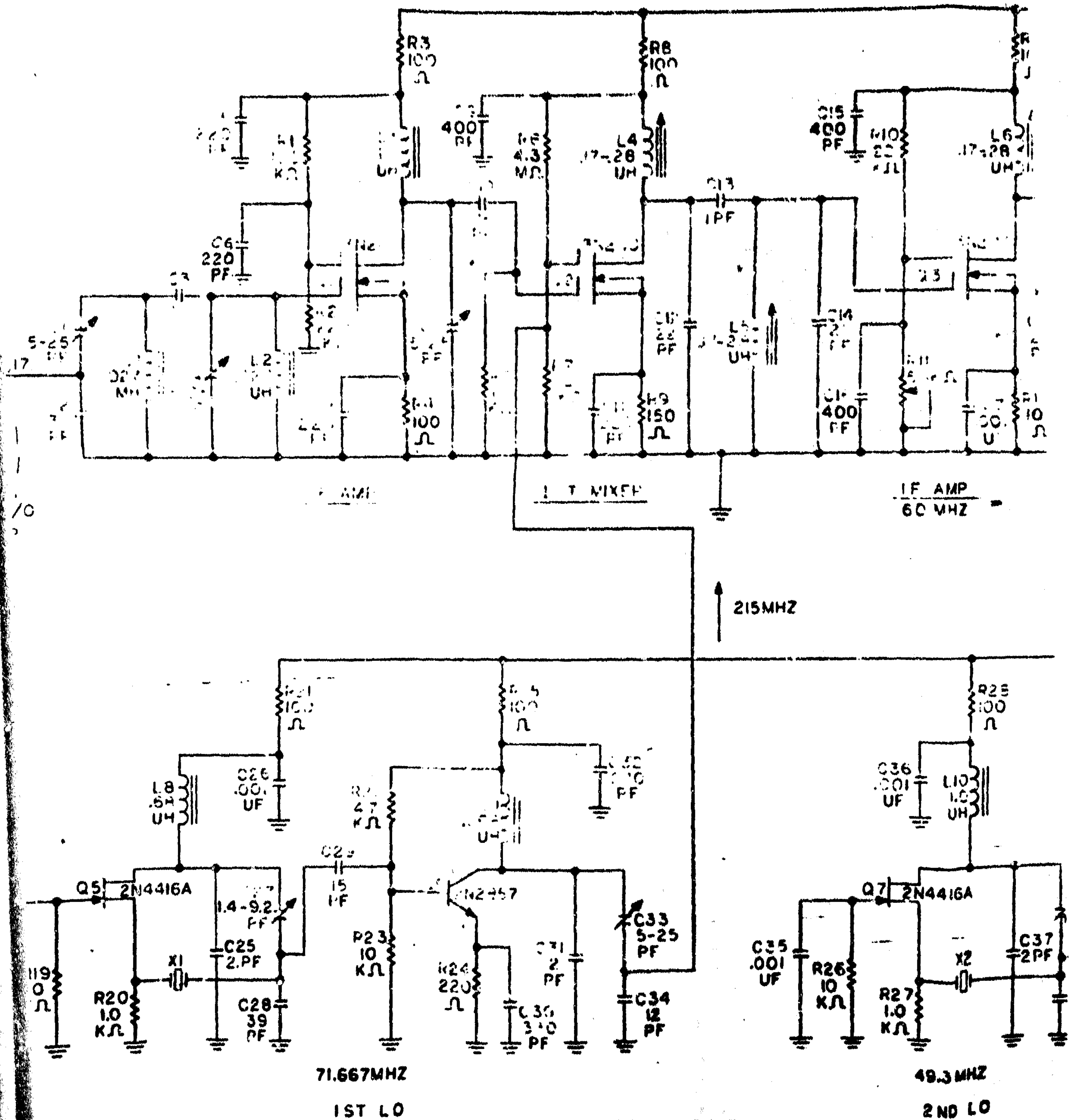
4.3.2.3 I-F BOARD

The 10.7 MHz If signal is fed through a narrow band crystal filter, Figure 4-7. The filter provides a 30 KHz bandwidth at the 3dB points. The 10.7MHz IF is amplified by Q1 and applied to a square law detector circuit CR1. The detector circuit output is transmitted as the 10 KHz or 8KHz 16 pulse train. This output is then passed through three amplifier limiter stages U1, U2, and U3. Limiter diodes CR2-CR3, CR4-CR5, and CR6-CR7 limit the positive and negative swing of the pulse train providing a maximum fixed level input to be applied to phase locked loop (PLL) detector U5. The PLL detector is adjusted so that a 10 KHz input signal results in a low output and an 8 KHz input results in a high output. The output pulse train therefore provides a high for a transmitted "1" and a low for a transmitted "0".


5-25
INPUT
FROM
ANT
P/O

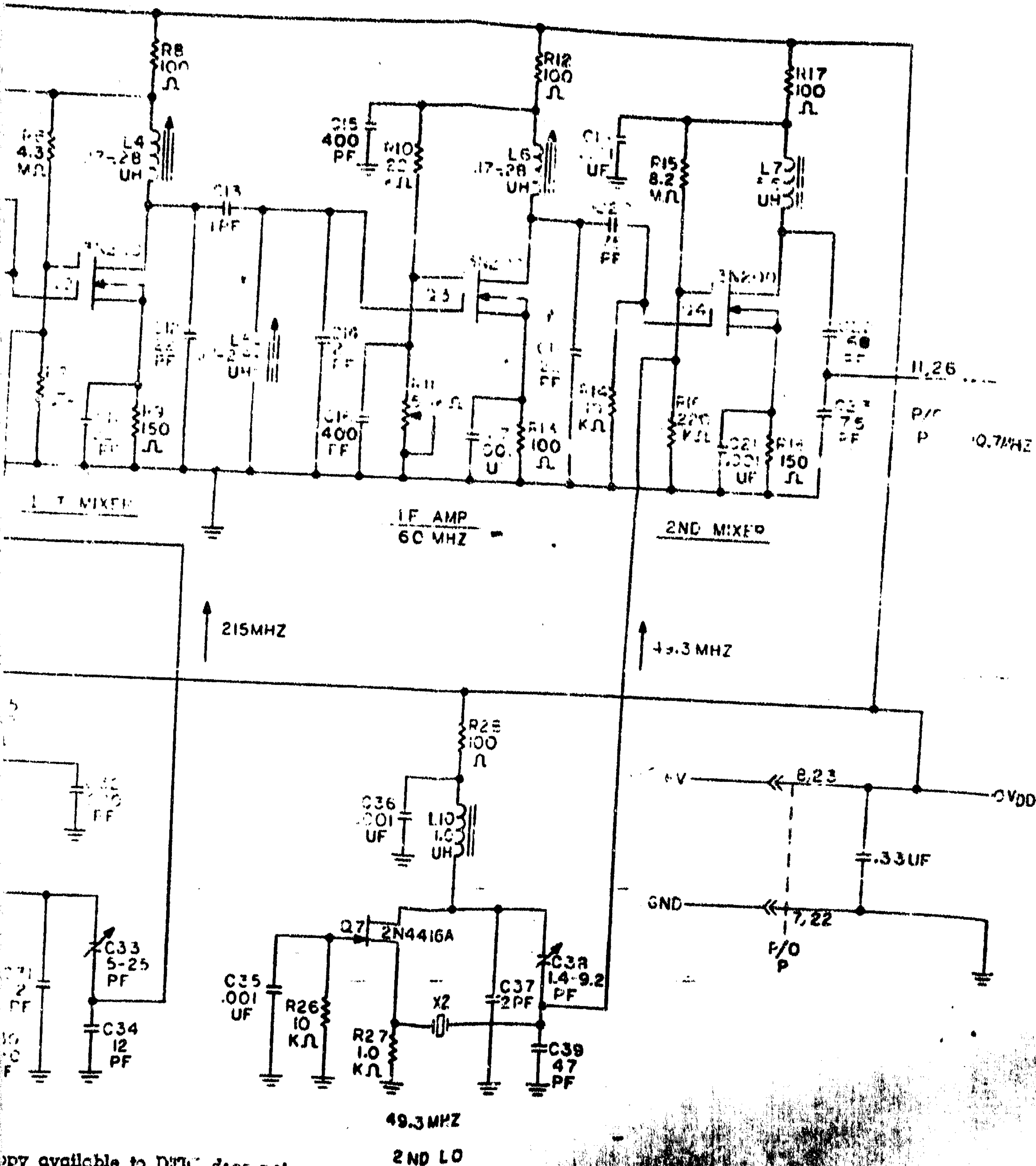

L8
Q5
2N4416A
C24
400
PF
R19
10
KΩ
R20
1.0
KΩ
X1

1


R3
100 Ω
R8
100 Ω
400 PF
4.3 MΩ
L4
.17-.28 UH
C13
1 PF
C15
400 PF
L6
.17-.28 UH
C6
220 PF
R4
100 Ω
R9
150 Ω
5-25 PF
22 PF
400 PF
IF AMP
60 MHZ
215MHZ
R21
100 Ω
R25
100 Ω
L8
.68 UH
C26
.001 UF
C36
.001 UF
L10
1.0 UH
Q5
2N4416A
1.4-9.2 PF
C25
2 PF
X1
R20
1.0 KΩ
C28
39 PF
C29
15 PF
47 KΩ
R23
10 KΩ
2N2857
R24
220 Ω
C31
2 PF
C33
5-25 PF
C34
12 PF
71.667MHZ
1ST LO
Q7
2N4416A
C35
.001 UF
R26
10 KΩ
X2
R27
1.0 KΩ
C37
2 PF
49.3 MHZ
2ND LO

①

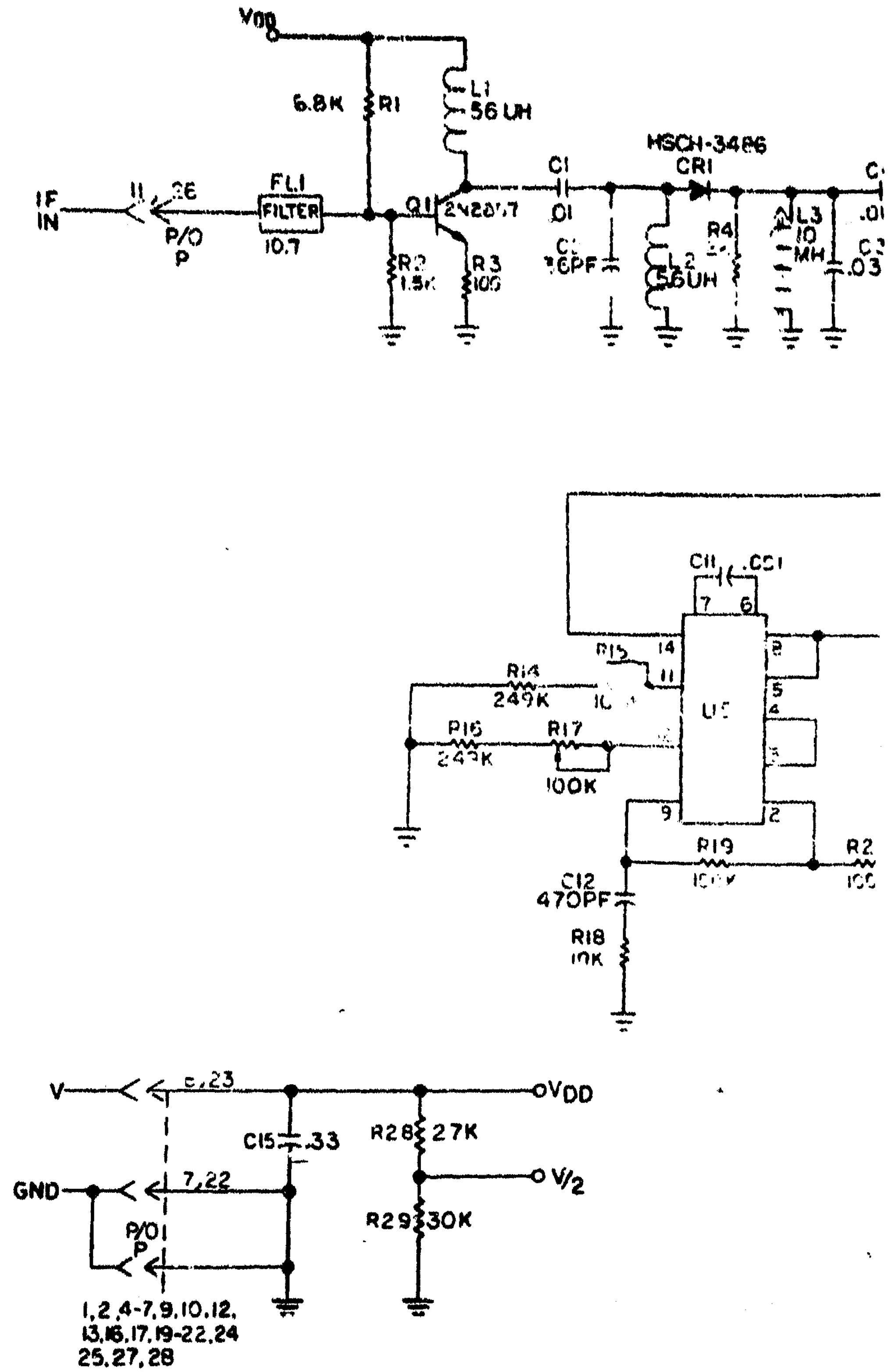
②



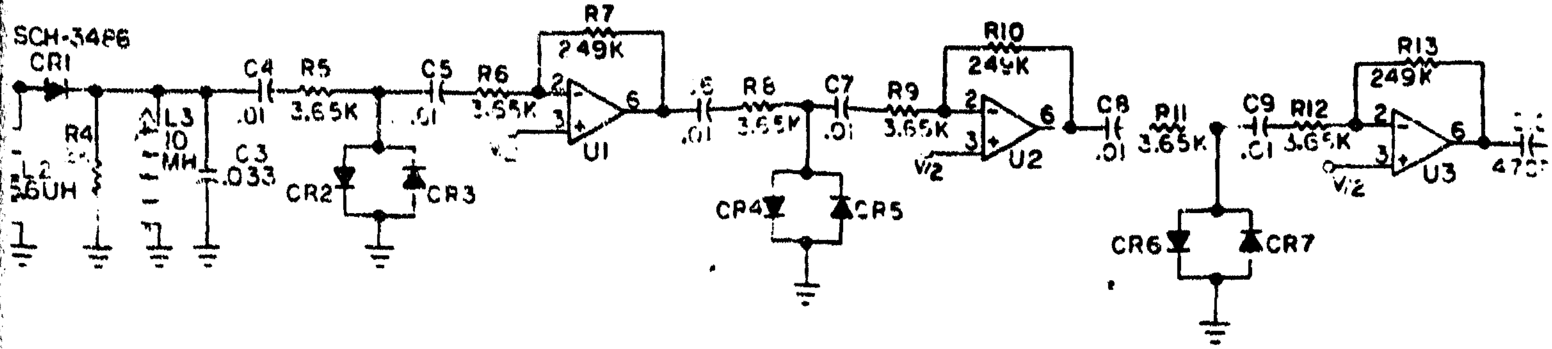
② 4-12

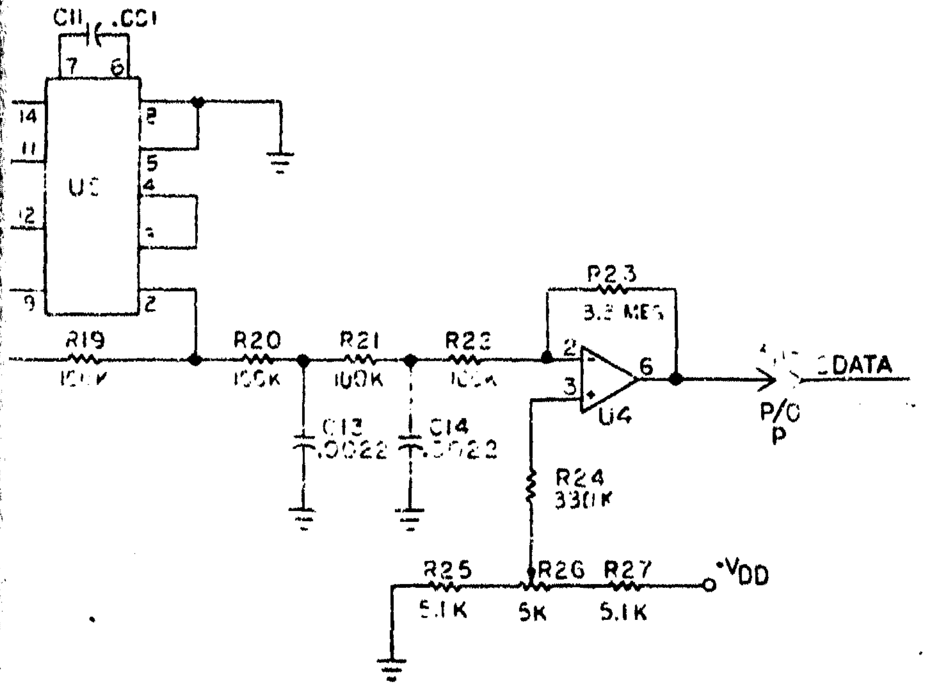
Receiver RF Schematic

③ 4-12


VDD
6.8K
R1
L1
56 UH
HSCH-3486
CR1
C1
.01
IF
IN
26
P/O
P
FL1
FILTER
10.7
Q1
R2
1.5K
R3
100
C2
56UH
R4
L3
10
MH
.03
C11
7
6
14
R15
11
R14
249K
R16
R17
100K
5
4
9
2
R19
R2
C12
470PF
R18
10K
V
VDD
C15
.33
R28
2.7K
GND
7,22
V/2
R29
30K
P/O
P
1,2,4-7,9,10,12,
13,16,17,19-22,24
25,27,28

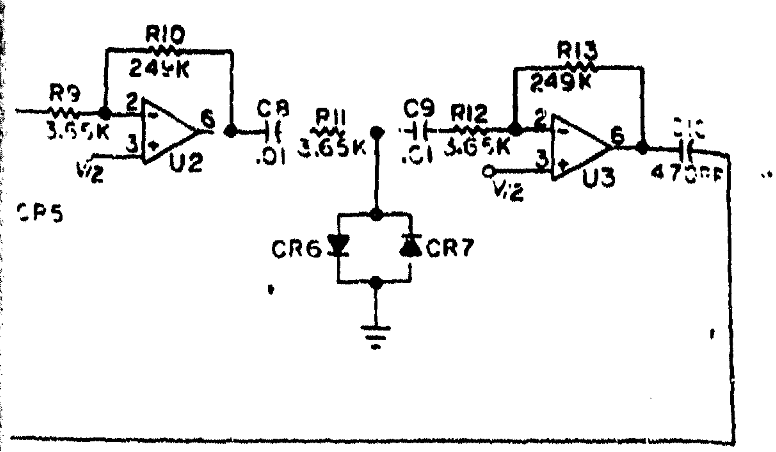
①


SCH-3486
CR1
R4
L2
5.6UH
L3
10
MH
C3
.033
C4
.01
R5
3.65K
C5
.01
R6
3.65K
CR2
CR3
R7
249K
U1
R8
3.65K
C7
.01
CR4
CR5
R9
3.65K
R10
249K
U2
V/2
C8
.01
R11
3.65K
CR6
CR7
C9
.01
R12
R13
249K
U3
V/2


C11
R19
R20
100K
R21
100K
R22
R23
U4
DATA
P/O
P
C13
.0022
C14
R24
330K
R25
5.1K
R26
5K
R27
5.1K
VDD

1

2



NOTES:

1 UNLESS OTHERWISE NOTED: ALL RESISTORS ARE IN OHMS 1/4W, CARBON COMPOSITION.

2 UNLESS OTHERWISE NOTED: ALL CAPACITORS ARE IN MICRO FARADS.

3 UNLESS OTHERWISE NOTED: ALL DIODES ARE IN4148 OR EQUIVALENT.

4 FOR U1, U2, U3, U4; VDD CONNECTED TO PIN 7, GND CONNECTED TO PIN 4.

5 FOR U5 VDD CONNECTED TO PIN 16

6 RESISTOR VALUES TO 2 DECIMAL PLACES ARE 1/8W, 1%

Figure 4-7. Receiver IF Schematic

3

4-13

This pulse train is shaped by the U4 circuit to provide a pulse train input to the serial/parallel converter which has sharp leading and trailing edges for processing.

Two additional signals generated by this circuit are the LTR and STR signals. The LTR signal is used to reset the decoder circuits and the STR signal is used on the decode board as a clock pulse for valid decodes.

These signals originate from the free running master clock. The 80 KHz master clock is counted down to 4.88 Hz at U4-15 and to 2.44 Hz at U4-1. The 4.88 Hz signal is counted down by 5 to provide a positive going STR output pulse about once every second at U1-3. The 2.44 Hz output at U4-1 is counted down by 16 at U6-4. The negative transition at U6-4 every 16 counts triggers U9, producing a positive LTR output pulse. Since the 2.44 Hz input represents the system rep rate, the LTR pulse occurs once for every 16 transmissions.

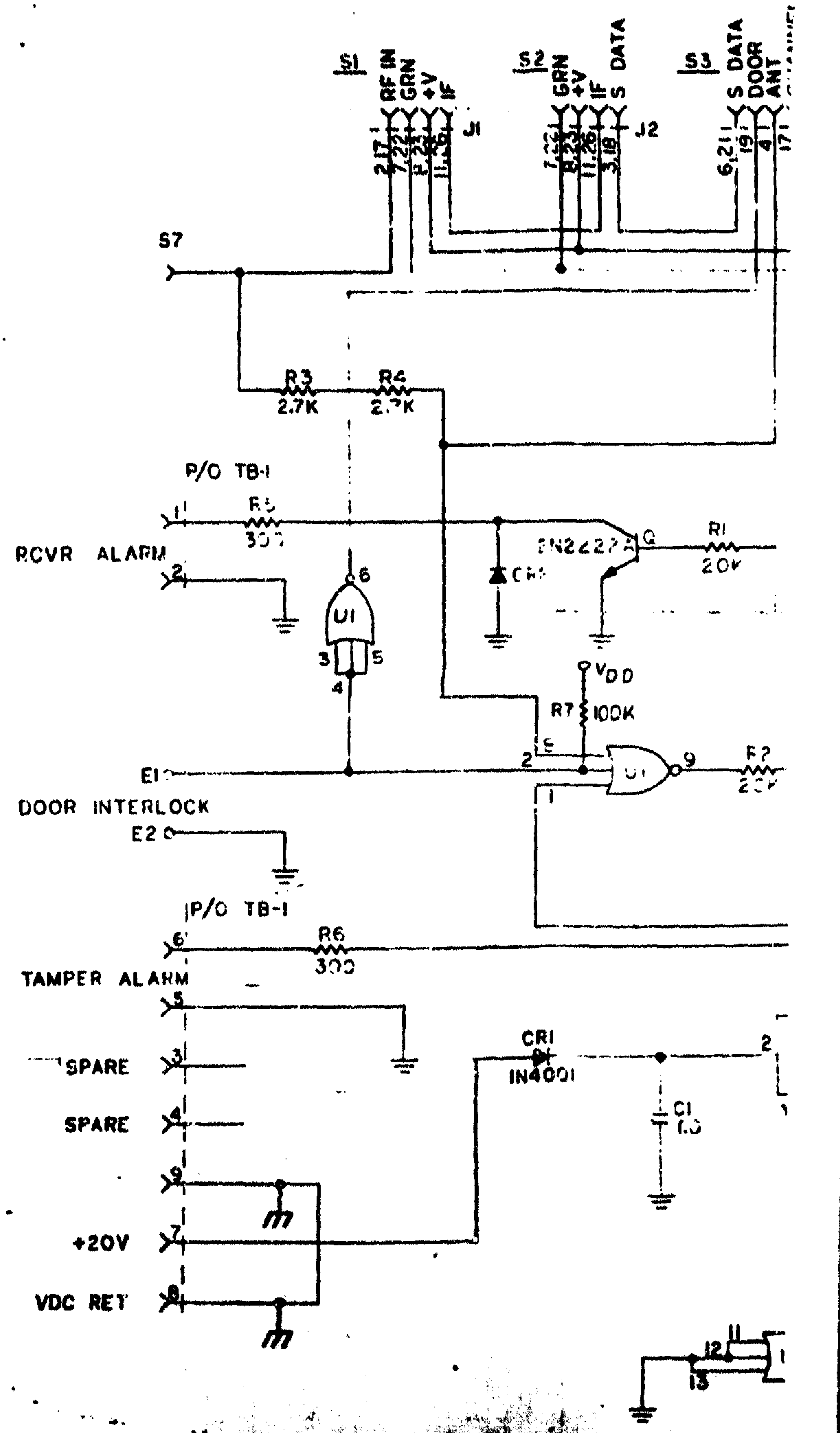
The tamper circuit is also on this board. If either the receiver antenna or cable are disconnected or if the receiver housing is opened, the one shot multivibrator U9 provides a 1.7 second pulse output at U9-6. This is routed through the driver circuit on the mother board to provide a high impedance (100K minimum) output when tampering occurs.

Also on the board is the one shot multivibrator U8 used for the channel alarm. If any of the decoder outputs (channel 1 through 6) are activated, a high is applied to N and gate U7. This results in a low at U7-13. The low triggers one shot U8 producing a 10 second positive pulse output at

U8-10. This pulse is routed to the driver circuit on the mother board Figure 4-8 to produce the high level (100K minimum) alarm output to an external control panel.

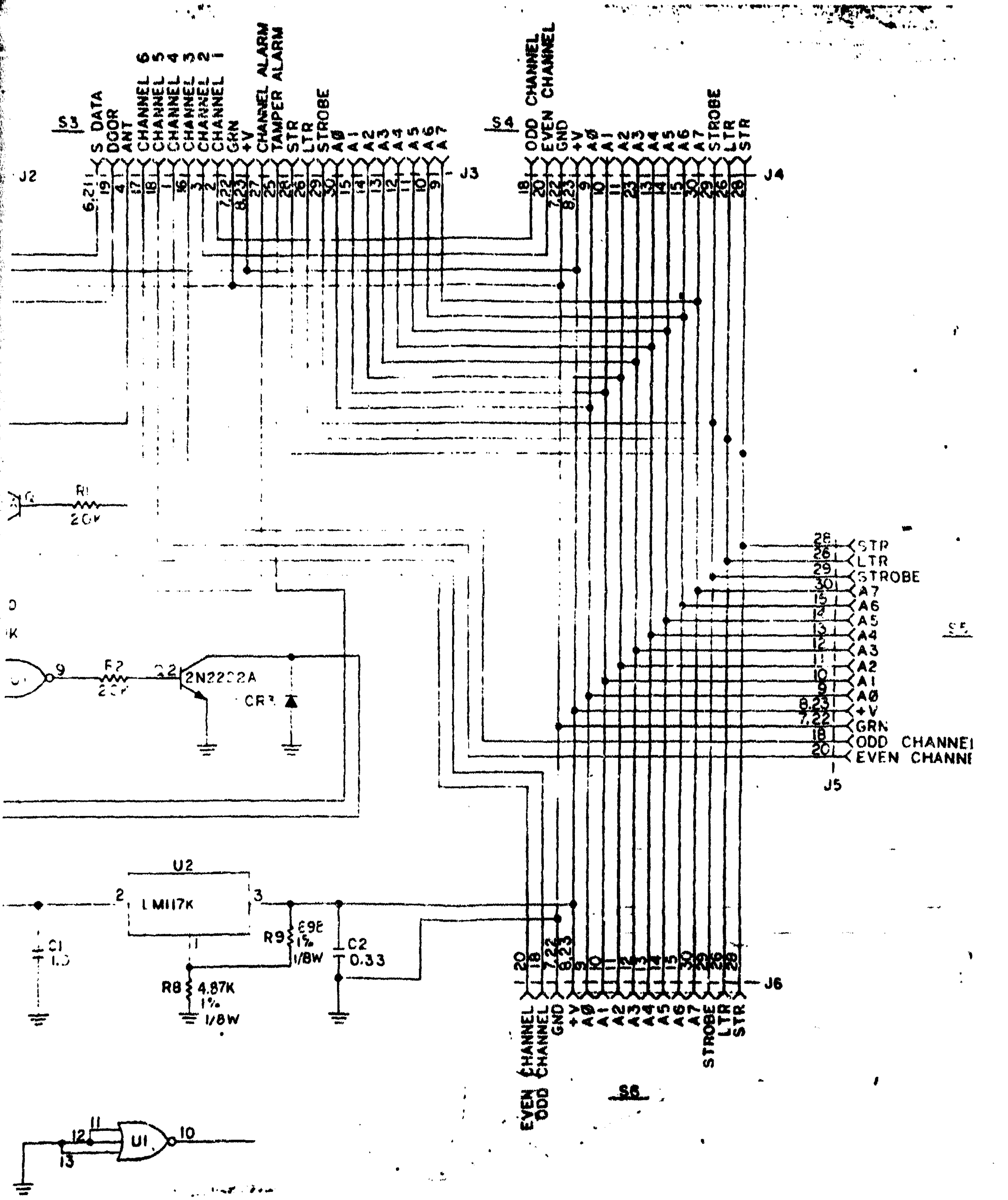
4.3.2.4 SERIAL/PARALLEL CONVERTER BOARD PULSE TRAIN DECODING

The serial pulse train input to the serial/parallel converter board, Figure 4-9, is applied to the integrator gate at U3-1, 2 and 8 and to shift register U10. Initially the shift registers U10 and U11 are inhibited by the high at U1-11. The 80 KHz clock output at U1-10 is free running. Figure 4-2 is the Decoder Timing Diagram. Remember that in a complete pulse train there are initially five "1"s, followed by one "0", followed by eight code pulses, followed by two "1"s. When the first five pulses of a pulse train appear, the input S data line is a high level. The initial five pulses can not be shifted into the shift registers U10 and U11 since the shift registers are inhibited. But these high level S Data signals are integrated by R12-C6 producing a positive rise in voltage across C6. After a period equal to approximately three consecutive pulses, C6 has charged to the threshold of gate U3 and the output at U3-9 swings low. Since the U1 latch circuit is already reset, the negative transition has no effect. At the end of the fifth pulse of a normal train, a "0" pulse is transmitted. This causes the S Data line to swing low at U3-8. The output at U3-9 swings high producing a positive pulse across R13 which sets latch U1. The low at U1-11 resets shift registers U10 and U11 and counter U2. The next 8 pulses (pulses 7 thru 14 of the transmitted train) represent data bits to be decoded and a ninth pulse (pulse 15 of the train) is used as a stop pulse.

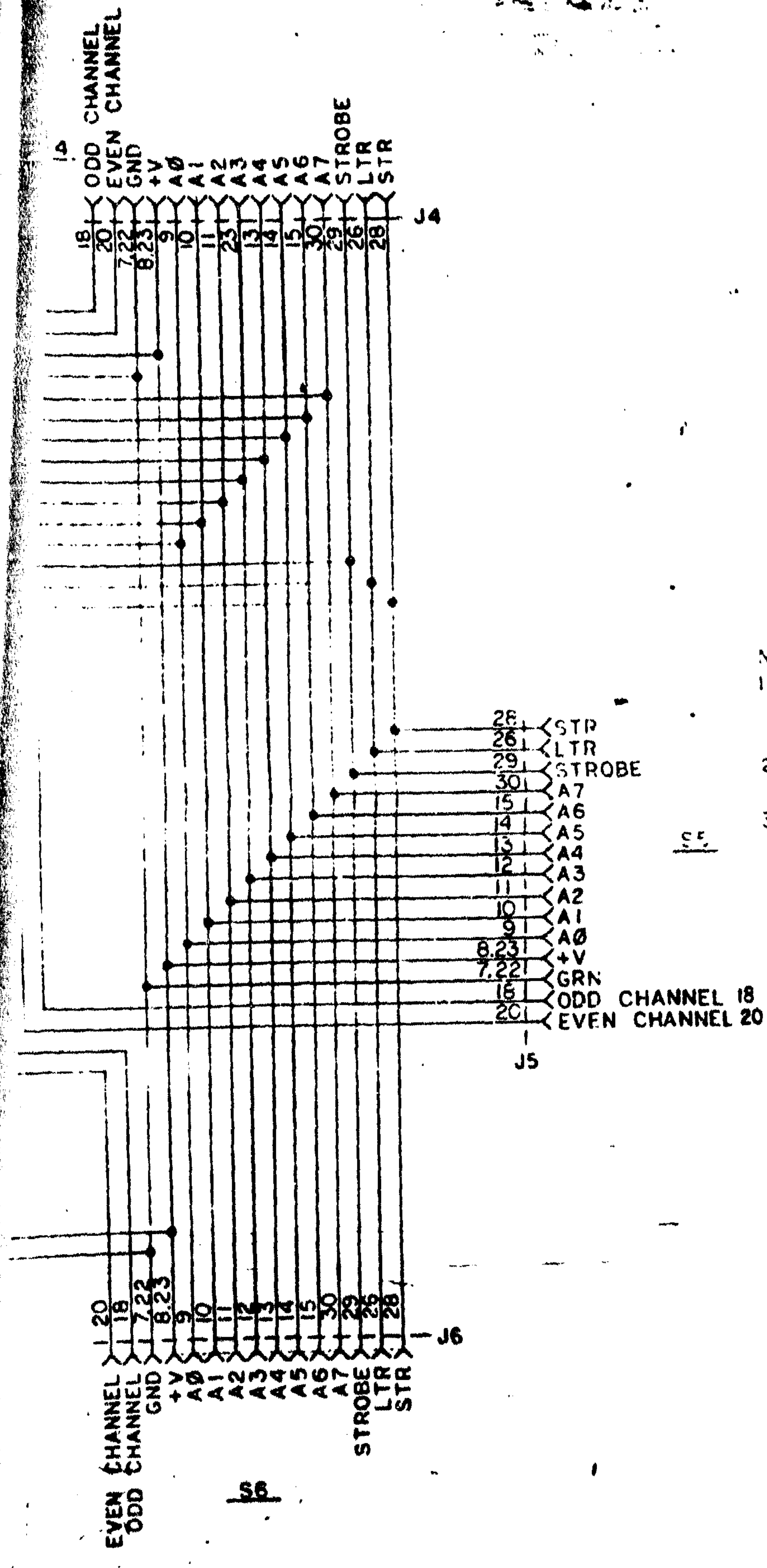


S1
RF IN
GRN
+V
IF
J1
S2
GRN
+V
IF
S DATA
J2
S3
S DATA
DOOR
ANT
S7
R3
2.7K
R4
2.7K
P/O TB-1
R5
300
RCVR ALARM
2N2222A
R1
20K
U1
VDD
R7
100K
E1
DOOR INTERLOCK
E2
R2
P/O TB-1
R6
300
TAMPER ALARM
SPARE
SPARE
CR1
IN4001
C1
+20V
VDC RET

4-16



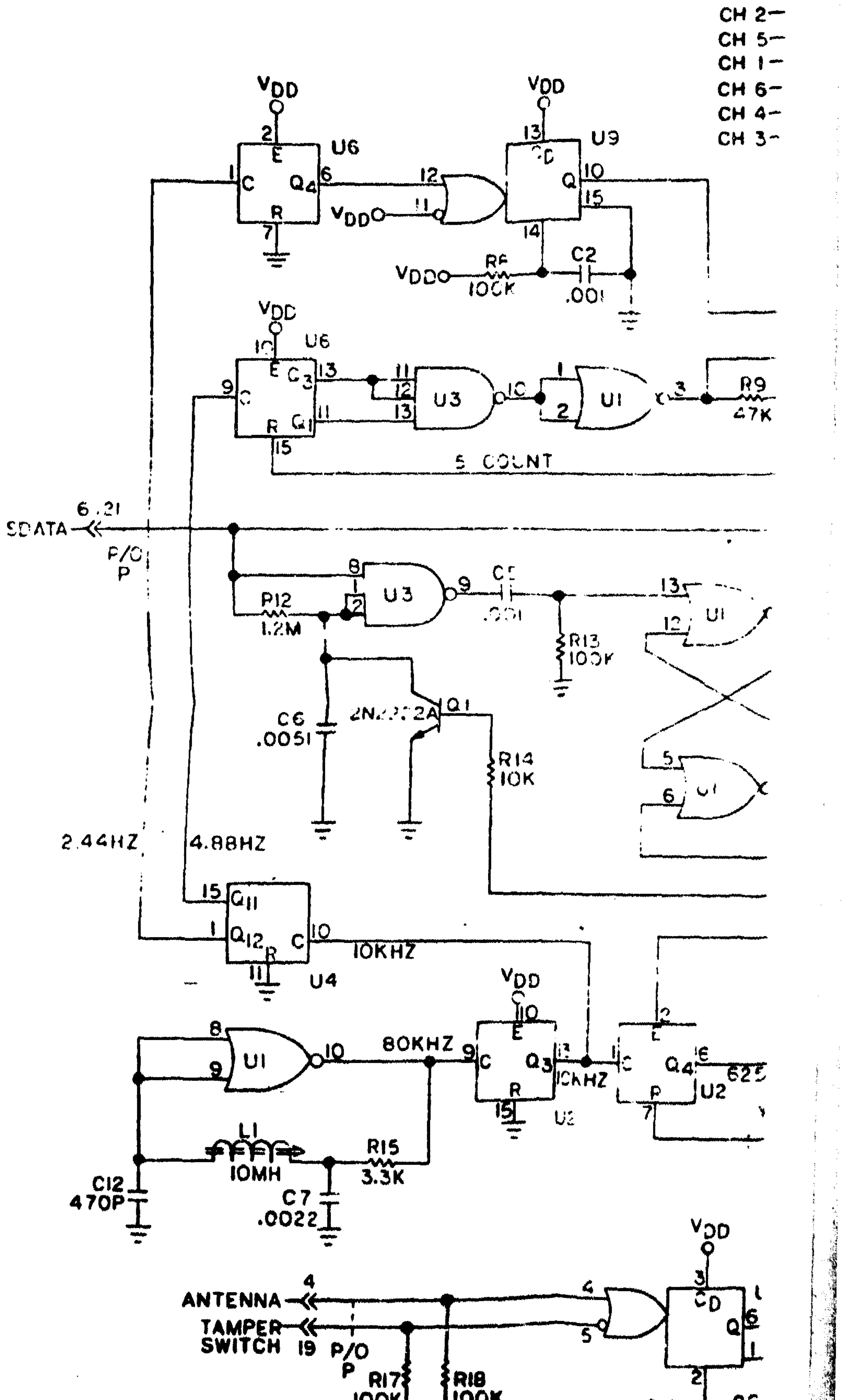
S3
S DATA
DOOR
ANT
CHANNEL 6
CHANNEL 5
CHANNEL 4
CHANNEL 3
CHANNEL 2
CHANNEL 1
GRN
+V
CHANNEL ALARM
TAMPER ALARM
STR
LTR
STROBE
A0
A1
A2
A3
A4
A5
A6
A7
J2
J3
S4
ODD CHANNEL
EVEN CHANNEL
GND
STROBE
LTR
STR
J4
R1
20K
R2
20K
2N2222A
CR3
ODD CHANNEL
EVEN CHANNEL
J5
U2
LM117K
R9
1%
1/8W
C2
0.33
C1
R8
4.87K
1%
1/8W
J6
S6
U1



NOTES

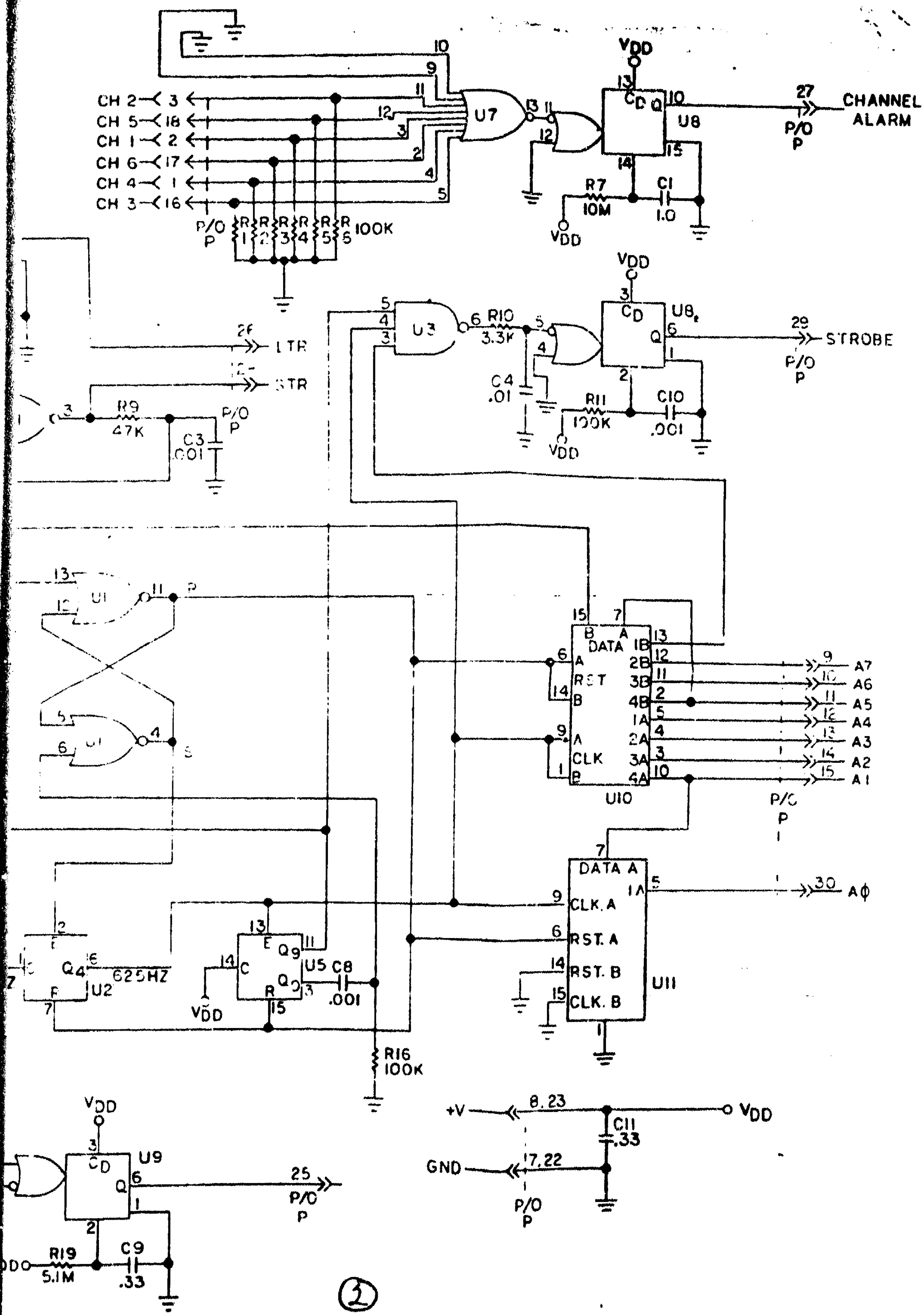
1. UNLESS OTHERWISE NOTED ALL RESISTORS ARE IN OHMS 1/4 WATT CARBON COMPOSITION
2. UNLESS OTHERWISE NOTED ALL CAPACITORS ARE IN MICRO FARADS
3. UNLESS OTHERWISE NOTED ALL DIODES ARE IN4148 OR EQUIVALENT.

Figure 4-8 . Mother Board Schematic ③

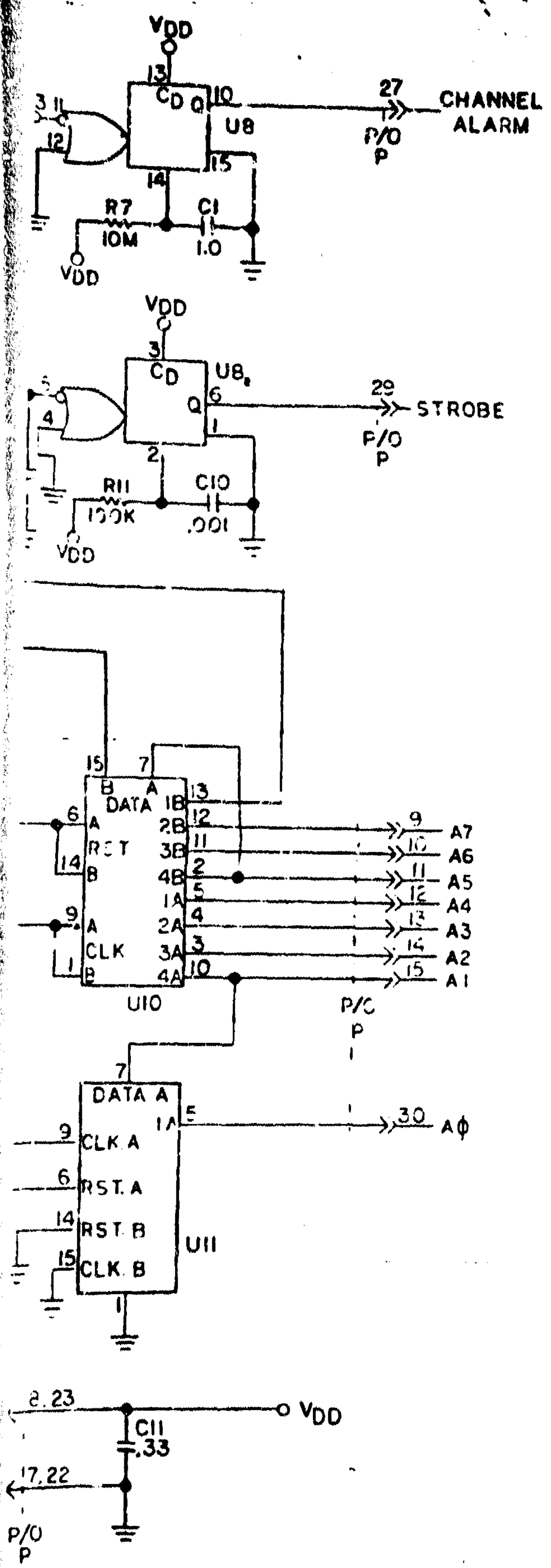

CH 2
CH 5
CH 1
CH 6
CH 4
CH 3
VDD
U6
U9
R8
100K
C2
.001
5 COUNT
U3
U1
R9
47K
SDATA
6, 21
P/O
P
R12
1.2M
C5
.001
R13
100K
C6
.0051
2N2222A
Q1
R14
10K
2.44HZ
4.88HZ
U4
10KHZ
80KHZ
U2
L1
10MH
R15
3.3K
C12
470P
C7
.0022
ANTENNA
TAMPER
SWITCH
R17
100K
R18
100K
R19
5.1M

4-17

①


CH 2 3
CH 5 18
CH 1 2
CH 6 17
CH 4 1
CH 3 16
P/O P
R1 R2 R3 R4 R5 R6 100K
U7
VDD
CD Q
U8
CHANNEL ALARM
27
R7 10M
C1 1.0
U3
R10 3.3K
C4 .01
U8
STROBE
29
R11 100K
C10 .001
LTR
STR
R9 47K
C3 .001
U1
DATA
RST
CLK
U10
A7
A6
A5
A4
A3
A2
A1
DATA A
CLK. A
RST. A
RST. B
CLK. B
U11
30
AΦ
U2
625HZ
U5
C8 .001
R16 100K
+V
8, 23
VDD
C11 .33
GND
7, 22
U9
25
R19 5.1M
C9 .33

Fi



NOTES:

1. UNLESS OTHERWISE NOTED, ALL RESISTORS ARE IN OHMS, 1/4 W, CARBON COMPOSITION
2. UNLESS OTHERWISE NOTED, ALL CAPACITORS ARE IN MICRO FARADS
3. UNLESS OTHERWISE NOTED ALL DIODES ARE 1N4 45 OR EQUIVALENT.

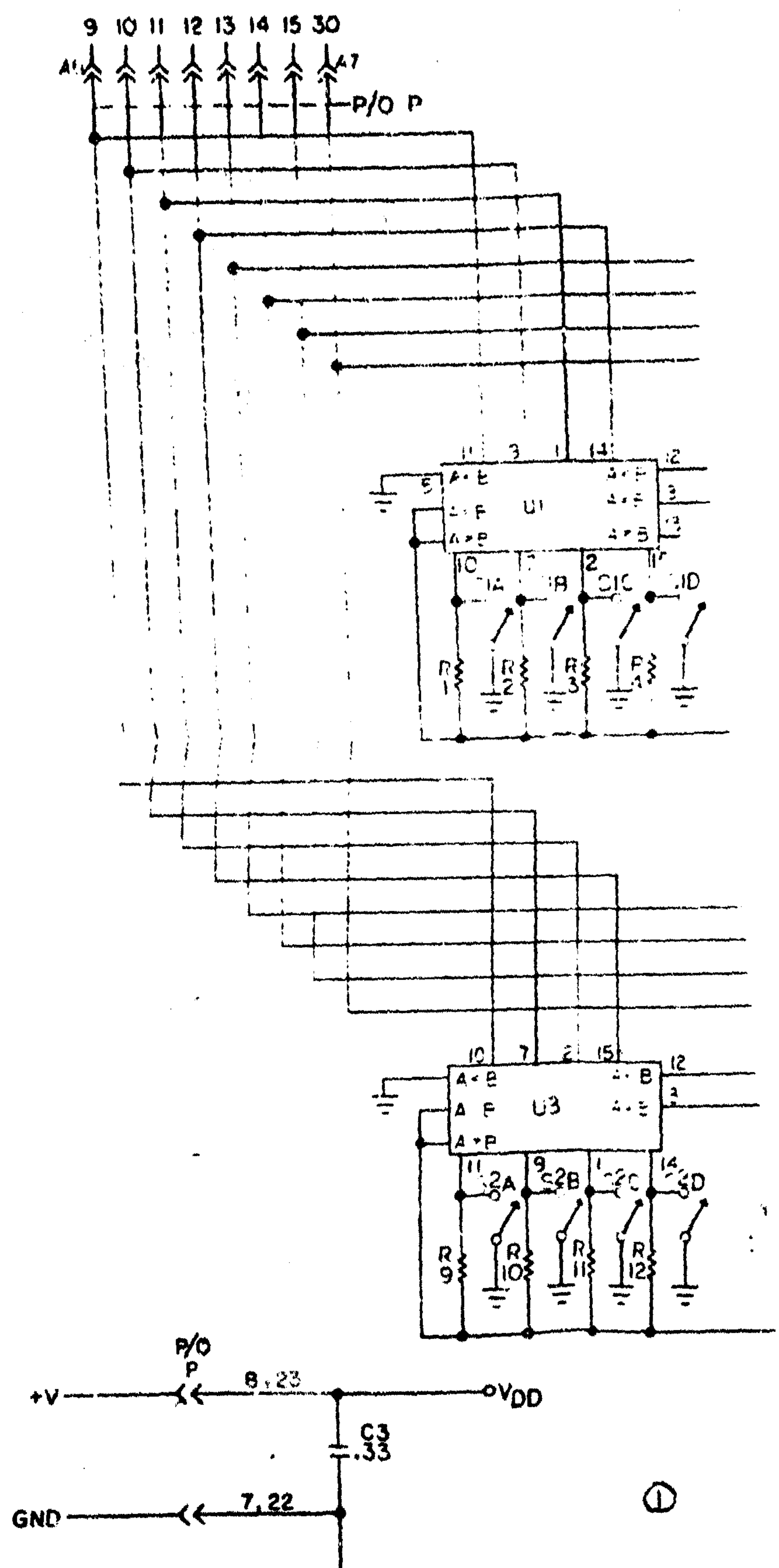
Figure 4-9. Serial/Parallel Converter Schematic

3

At this time the high at U1-4 enables counter U2 at pin 2. Counter U2 at pin 6 provides a 625 Hz clock pulse to the shift register U10 and U11. The clock pulse shifts the pulse train represented by highs and lows on the S data line into the shift register. At the end of the ninth clock pulse, U5 pin 11 swings high. This turns on Q1 discharging C6 and inhibiting the input gate at U3-2. This same high is applied to gate U3 at pin 5 as one high. A second high occurs from clock pulse 9 and the third high from the ninth pulse (stop pulse) shifts into the shift register. This pulse from U10-13 causes Nand Gate U3 at pin 6 to produce a negative output which is differentiated by R10-C4 to trigger the strobe gate. The strobe gate monostable provides a 100 microsecond positive pulse output which is applied to the decoder board. The next clock pulse (pulse 10) produces a positive output pulse at U5-3 which resets the U1 latch inhibiting the clock output and the shift registers.

4.3.2.5 DECODER BOARD

The decoder board Figure 4-10 receives the parallel format code output pulses A_0 through A_7 from the serial to parallel converter board. These pulses are applied to two comparator circuits. Comparators U1 and U2 are in the odd channel number circuit and U3 and U4 are in the even number channel circuit. Both channels operate identically. For discussion purposes, refer to the odd channel. The code sequence on input lines A_0 through A_7 is compared to the code set on switch assemblies S1 and S2. If a simultaneous match at all positions occurs, the A = B output will be a high. Any mismatch produces a low output. This is applied as one input of And gate U7. At this time a positive strobe pulse is also applied to the And gate. Thus if a decode match is present in the



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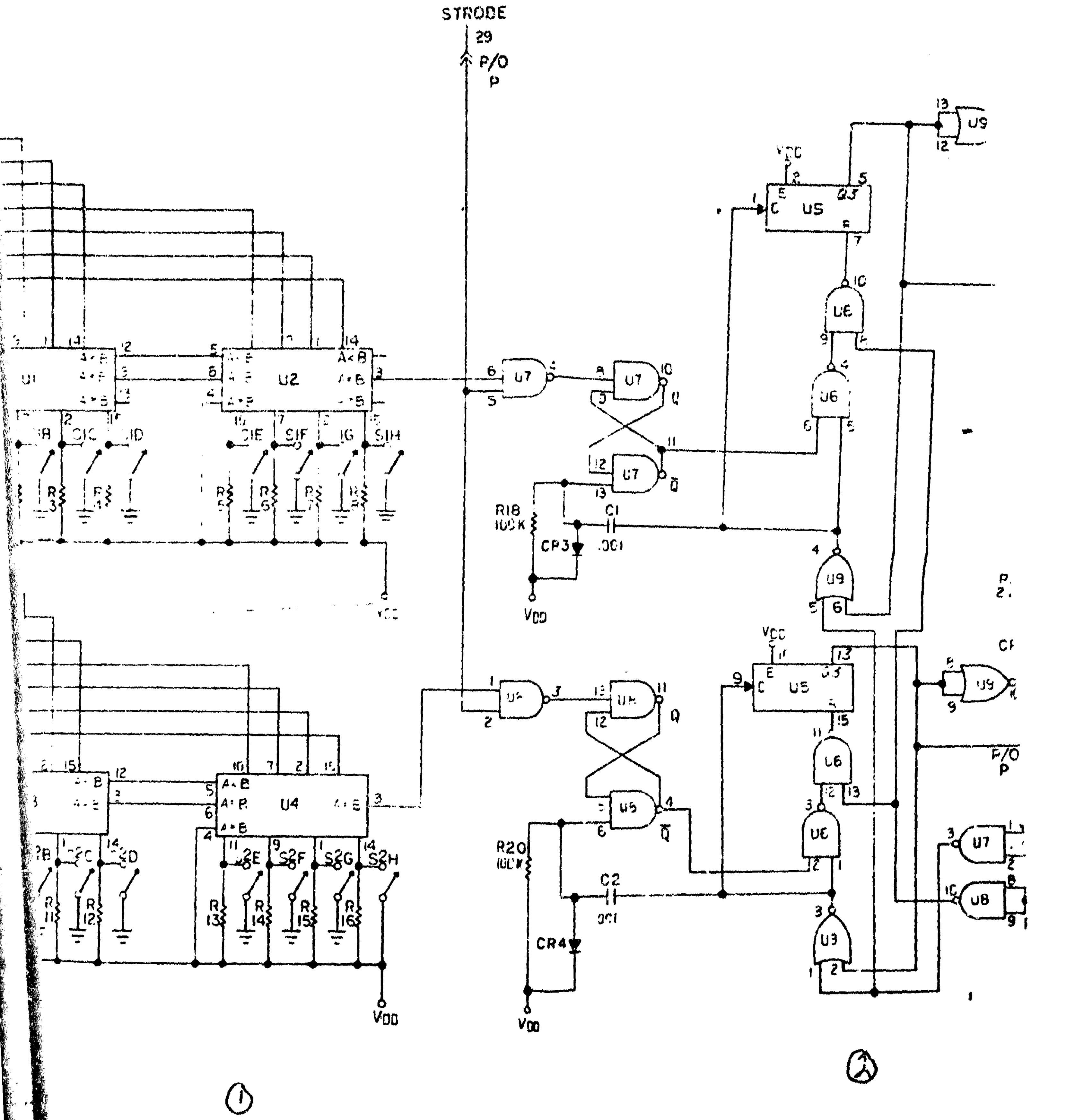
STRODE
29
P/O
P
U1
U2
U4
U5
U6
U7
U8
U9
R18
100K
CR3
C1
.001
VDD
R20
100K
C2
.001
CR4
Q
S2E
S2F
S2G
S2H
S1E
S1F
S1H
VDD
①
②

4:19

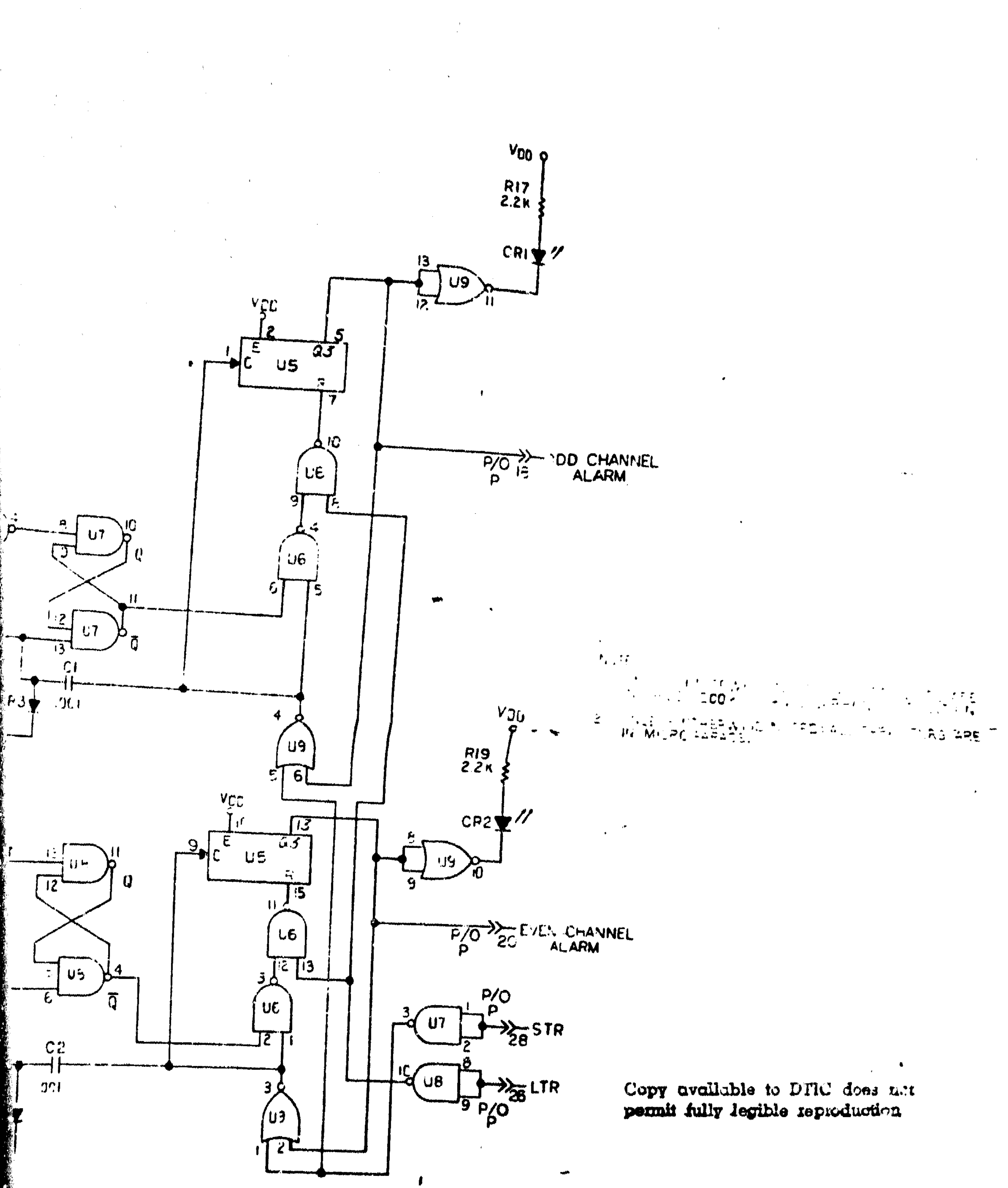

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Figure 4-10. Decoder Schematic

comparator at the time the strobe is generated the And gate U7 produces a low output for the 10 microsecond duration of the strobe.

The low output at U7-4 sets the latch at U7-8. The low output at U7-11 inhibits the counter U5 reset line by applying a low at U6-6. The STR pulses are then routed to counter clock input U5-1 through Or gate U9 pin 5. The STR also resets the latch at U7-13. The STR pulses are counted by counter U5. The circuit is arranged so that a valid code sig-al must be received before the next STR pulse, otherwise counter U5 is reset. If four or more consecutive STR pulses are counted, the output from the counter at U5-6 is a high. This turns on the LED indicator CRI through inverter U9, applies a high to the odd channel decode line to activate the alarm circuit and also provides a reset through U9-6 to reset the latch circuit. The LTR pulse is used to reset the counter at the end of every 16 pulse trains.

Thus if the counter has not received at least three STR pulses indicating three valid decodes within 16 transmission cycles the counter is reset to 0 and starts counting over. This reduces the possibility of stray noise pulses initiating a decode output.

SECTION 5

MAINTENANCE AND REPAIR

5.1 INTRODUCTION

This section contains information and instruction covering disassembly, repair, and preventive and corrective maintenance for the Duress Sensor equipment. Preventive maintenance consists primarily of cleaning the equipment and should be performed as often as operating conditions require. Corrective maintenance consists of troubleshooting, alignment and tuning adjustments, which are designed to aid in maintaining instrument operation within specifications. Section 4, Theory of Operation, is an important supplement to the troubleshooting section since a thorough knowledge of equipment theory is indispensable to troubleshooting.

CAUTION

Troubleshooting should only be done by qualified technical personnel with proper equipment to make basic alignment and tuning adjustments. Operators should not tamper with internal adjustments, as doing so may lead to malfunction of the equipment and any attempt to open the equipment will set off the tamper alarm.

5.2 TEST EQUIPMENT

The equipment recommended for troubleshooting and alignment of the PDS System is listed in Table 5-1. If the recommended equipment is not available, other equipment having equivalent specifications may be used by skilled personnel.

Table 5-1. Recommended Test Equipment

EQUIPMENT NOMENCLATURE	RECOMMENDED EQUIPMENT TYPE, Model No.	FUNCTION
Volt-ohm-meter (2)	Simpson Model 260, 20,000 ohms per volt minimum input resistance	Troubleshooting Alignment
Audio Generator	Hewlett Packard Model 200 CD	Troubleshooting Alignment
Oscilloscope	Tektronix Model 545A	Troubleshooting Alignment
RF Voltmeter with RF Probe	Hewlett Packard Model 411A Vacuum Tube Voltmeter with Type 11023A UHF low capacity probe	Troubleshooting Alignment
Signal Generator (3)	Hewlett Packard Model 606A	Troubleshooting Alignment
Tuning Tool Set	Fiber or Plastic	Alignment
Frequency Counter	Hewlett Packard Model 5245L Electronic Counter	Alignment
Spectrum Analyzer	Nelson Ross Electronic Plug-In	Alignment

5.3 ACCESS

5.3.1 GENERAL

The following procedures may be used to gain access to components of the transmitter or receiver units for changing crystals, setting codes, changing transmitter batteries and for general maintenance.

5.3.2 TRANSMITTER

CAUTION

Opening of transmitter for maintenance will initiate an alarm.

1. Loosen the two screws located on the housing of the unit, Figure 5-1.

NOTE

The printed circuit board will remain attached to the front cover with connecting wires to switches and batteries attached within the case.

2. Lift back housing off being careful not to break connecting wires and lay sections next to each other. The transmitter can now be serviced.

5.3.3 RECEIVER

CAUTION

Opening the access cover of the receiver for maintenance will initiate the tamper alarm.

a. Remove the two screws on the right edge of the receiver access door and swing door open.

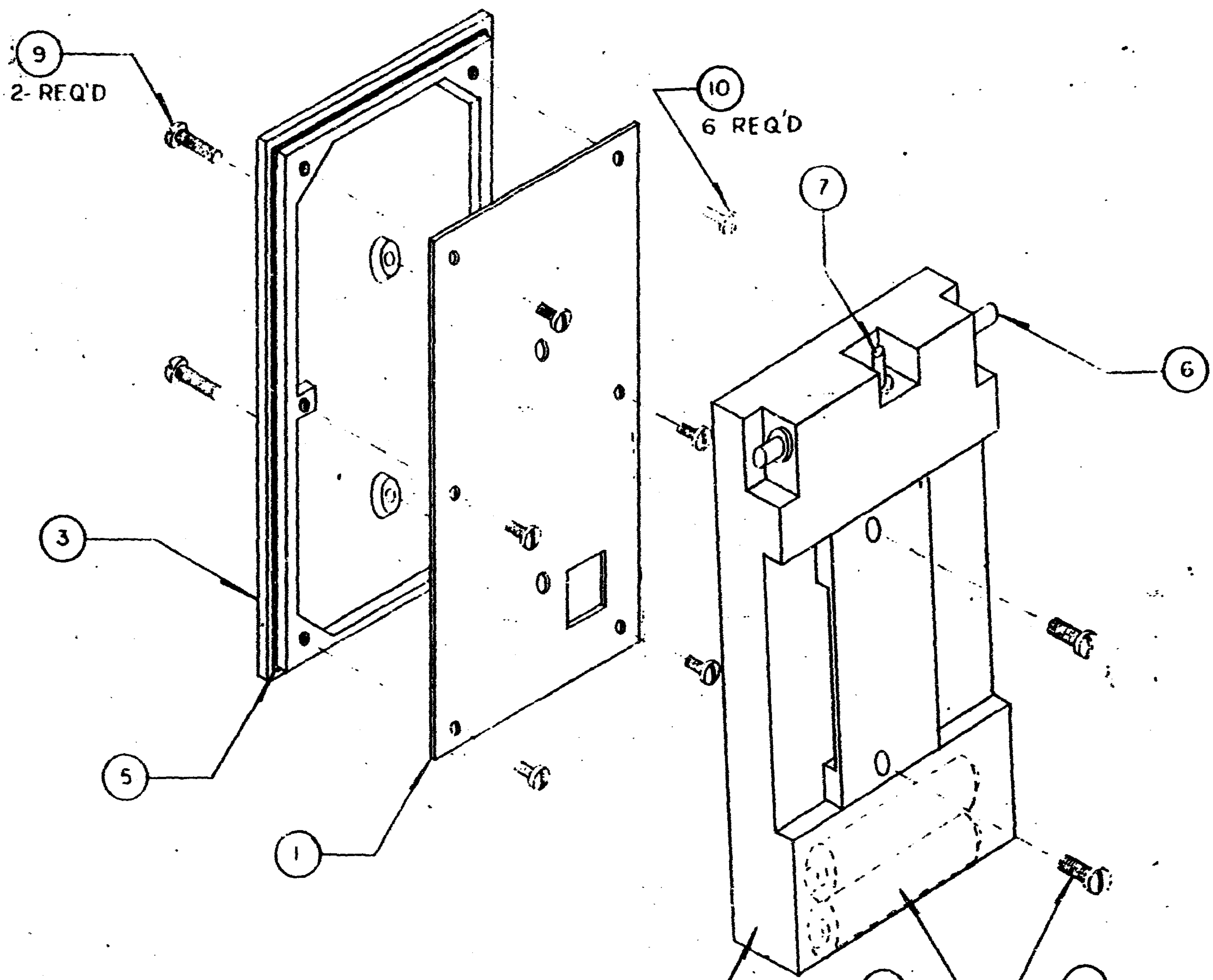

Figure 5-1. Transmitter Access

b. Pull out on tamper switch, (Figure 5-2), to place receiver in the "service" mode.

c. If access to printed circuit cards is required remove the six screws holding the printed circuit board hold-down plate and remove plate. The receiver can now be serviced.

5.4 DISASSEMBLY

5.4.1 TRANSMITTER

The transmitter contains only one printed circuit board. The board is attached to the front cover by screws. To remove the printed circuit board completely from the cover, remove the screws. Procedures for removal of the two push-button switches and the covert switch connector are obvious upon inspection.

5.4.2 RECEIVER

5.4.2.1 PRINTED CIRCUIT CARD REMOVAL AND REPLACEMENT

a. Provide access to the circuit cards by performing the procedure in paragraph 5.3.3.

b. Grasp the circuit card to be removed near the top and bottom and pull the circuit card straight out.

c. Insert the replacement printed circuit card into the slots of the card rack with the component side of the board toward the left side of the unit. The proper location for each board is illustrated in Figure 1-3.

5.4.2.2 MOTHER BOARD REMOVAL AND REPLACEMENT

a. Provide access to the printed circuit mother board by performing the procedure in paragraph 5.3.3.

b. Remove the printed circuit cards from the card rack.

c. Disconnect the receiver antenna lead-in cable at the bottom of the housing.

d. Label wires, then disconnect the power input leads from the terminal strip at the top of the receiver.

e. Label and disconnect the alarm output wires from the terminal strip.

f. Remove the eight screws, (four on each side) attaching the mother board to the housing.

g. Lift mother board with card rack attached, out of housing.

NOTE

If mother board is to be replaced, remove card cage and install card cage on new mother board as described below.

h. Disconnect tamper switch wires from terminals E1 and E2. Tamper switch should remain attached to the card rack.

i. Remove six screws from under side of mother board which attach off of the mother board.

j. Install card cage with tamper switch attached to new mother board with six screws. Tamper switch must be toward right side of mother board.

k. Solder tamper switch wires to mother board at terminals E1 and E2.

l. Reinstall mother board into housing.

m. Reinstall printed circuit board.

NOTE

Be sure decoders are properly set to the correct code.

n. Reinstall circuit board hold-down plate with six screws.

o. Reconnect alarm wires and power input wires to terminal strip.

p. Close access cover and attach with two screws.

5.5 CLEANING

The transmitter and receiver units should be cleaned periodically to remove dust, grease and other contamination. The exterior surfaces should be cleaned with a soft cloth dampened in a mild solution of detergent and water.

CAUTION

Do not use solvents to clean transmitter or receiver units

5.6 CRYSTAL REPLACEMENT

5.6.1 TRANSMITTER CRYSTAL

The following procedures should be followed for installation of crystals in the master oscillator circuit. The unit is shipped with a 68.75MHz crystal for operation at 275MHz. If a different operating frequency is desired, determine the required crystal frequency by the following formula.

$$F_c(\text{MHz}) = \frac{F_o(\text{MHz})}{4}$$

F_c = crystal frequecncy

F_o = output frequency

The crystal is mounted on the rf section of the printed circuit board. After replacing a crystal, refer to the transmitter alignment paragraph for properly tuning the transmitter.

5.6.2 RECEIVER CRYSTALS

The receiver contains two crystals. The first local oscillator crystal frequency depends on the frequency of the incoming signal. The second local oscillator crystal is fixed at 49.3 MHz. Both crystals are located on the receiver rf amplifier printed circuit board.

The first local oscillator crystal frequency is determined using the following formula.

$$F_c(\text{MHz}) = \frac{(Fr-60)\ \text{MHz}}{3}$$

Thus for the frequency of the unit as shipped (275MHz) the crystal frequency is:

$$F_c(\text{MHz}) = \frac{(275-60)\ \text{MHz}}{3} = \frac{215\ \text{MHz}}{3} = 71.667\text{MHz}$$

After replacing a crystal refer to the receiver alignment procedure paragraph for properly aligning the receiver circuit.

5.7 TROUBLESHOOTING

5.7.1 RECEIVER ANTENNA SYSTEM

Antennas that have deteriorated because of weather or accidental damage can seriously affect the performance and reliability of the receiver. Poor operation is usually caused by faulty antenna systems. Check for obvious opens or shorts in the transmission line. Repair or replace line.

Check to see if the antenna is broken or if the insulator between the ground plane and the antenna has a build-up of dirt, snow or ice. If the problem is dirt, grease or grime, the antenna insulator base should be wiped clean. Snow or crusts of ice should be removed regularly.

5.7.2 TRANSMITTER SYSTEM

The PDS Transmitter should be activated periodically to verify proper operation. If the PDS receiver does not provide an output in response to the transmitter verify that the code setting of the transmitter and receiver are the same. If they are not, set the code switches in both the receiver and transmitter to the same setting and check for an alarm response. If the receiver and transmitter are set to the same code, change the code switched to first all "on" and then all "off" and recheck for alarm initiation. If the alarm still does not function, connect a scope probe to R of the IF board in the receiver in order to monitor the 10.7 MHz IF frequency. In response to the transmitter the 10.7 MHz wave form out of the IF should be clean and symmetrical. The duration of this signal should be 23 rms min. The presence of this waveform indicates that the receiver is receiving the transmitted signal. If the receiver is operating properly but the transmitter is not and the IF signal has the proper waveform, then the transmitter is not transmitting a coded modulated signal in accordance with the code switch. With a PDS antenna connected to a spectrum analyzer and the transmitter standing next to the antenna ground plane approx 1" from the vertical rod, the output transmitter power should be at least 0 dBm.

If the transmitter output power is sufficient then either the code switch is faulty or the RF waveform of the transmitter may be distorted. (Usually running a code identification test with the code switches all open then all closed can isolate the fault to the coded switch.) For eliminating the distortion of the transmitter waveform, refer to section 5.8.1.3 step 13 of Final Alignment procedure for the transmitter.

The transmitter Initial Alignment procedures may be utilized to isolate faults within the transmitter RF section by observing where in stage-by-stage alignment procedure the proper signal is not obtained.

CAUTION!! ALIGNMENT ADJUSTMENTS SHOULD NOT BE ATTEMPTED UNTIL ALL OTHER FAULT ISOLATION PROCEDURES HAVE BEEN EXHAUSTED!

5.7.3 RECEIVER SYSTEM

5.7.3.1 RECEIVER PCB LEVEL

In conducting trouble shooting procedures to isolate faults to the printed circuit board level, the most convenient aid is a properly functioning PDS transmitter unit and a voltmeter. The voltmeter is necessary to determine if the +10 volts is available from the voltage regulator IC on the mother board. Assuming the supply voltage to the PCB's is within the specified range of 10 volts $\pm$ 5%, the most expedient way to isolate trouble to the PCB level is by board substitution.

The following is a procedure for rapidly isolating trouble when a full set of spare boards is available:

1. Remove the sheet metal cover to the PCB card cage.
2. Remove the six plug-in PCB's from the card cage and replace them with good boards. Only one channel decoder board is necessary for fault isolation.
3. Remove shorting plug from the covert switch input of the transmitter to initiate the output signal.
4. Set the code pattern on both D.I.P. switches to duplicate the code pattern of the transmitter.
5. After a maximum period of 15 seconds, the two channel alarm L.E.D. indicators of the CHANNEL DECODER board should light. This 15 second period allows for the worst-case combination of transmitter re-cycling time and receiver alarm reset time. In general, the alarm indicators will activate within a smaller time interval after the proper code pattern has been set. If an alarm condition is not obtained,

and the replacement boards are known to be good, the MOTHER BOARD is probably at fault. Either the supply voltage or PCB socket interconnector must be suspect.

The MOTHER BOARD may be changed by removing the 8 screws securing it to the sheet metal enclosure, the external wires from the terminal block, and the RF coax connected to the signal input connector.

The board is disassembled from the card cage by removing the 6 screws on the bottom of the board, detaching the miniature coax connector, and disconnecting the two wires leading from the board to the screw terminals on the tamper switch.

6. If the two channel alarm indicators activate, the channel decoder board should be inserted in the other two decoder board slots to ensure that those positions on the MOTHER BOARD are in working order.

7. When the receiver has been checked with the spare boards, the spare boards should be replaced, one at a time, commencing with the R.F. AMPLIFIER board, until the board with the fault has been located.

5.7.3.2 TROUBLESHOOTING RECEIVER TO PCB LEVEL WITHOUT THE USE OF SPARE BOARDS

In conducting trouble shooting procedures to isolate faults to the printed circuit board level without the use of spare boards, a properly functioning PDS transmitter unit and an oscilloscope are required. The transmitter is utilized as a source with an output signal of proper

characteristics to exercise each receiver plug-in board. The oscilloscope is utilized to determine if the correct output is obtained from each board.

5.7.3.2.1 RF AMPLIFIER BOARD

1. Remove the sheet metal cover from the receiver card cage.

2. With the oscilloscope input set to a D.C. mode, measure the DC voltage supplied to the printed circuit boards by the voltage regulator I.C. The voltage may be measured between ground reference (card cage) and the case of the regulator (LM117K). The voltage should be + 10 volts $\pm$ 5%.

3. Remove all except the RF amplifier plug-in board and activate the PDS transmitter unit by removing the shorting jumper for the covert switch input.

4. Remove tip from oscilloscope probe (TEKTRONIX P6062B), and insert probe tip into pin 26 of the connector adjacent to the RF board. Connect the oscilloscope probe tip to ground reference. The pulsing RF envelope of the transmitter should be visible on the oscilloscope screen. For a transmitter unit held within 30 to 50 feet of the receiving antenna, and provided there are no intervening metallic structures, the output amplitude of the RF pulse should be at least a few tenths of a volt. If no pulsing output is observed, replace the RF amplifier board.

5.7.3.2.2 IF Demodulator Board

Assuming that the PDS Receiver unit has been determined to be working through the RF board, and that a functioning transmitter unit is available, the IF - DEMODULATOR BOARD may be tested.

1. Insert the IF DEMODULATOR board into the socket adjacent to the RF AMPLIFIER board. The remaining boards in the receiver unit should not be plugged in.

2. Insert oscilloscope probe tip (TEKTRONIX P6062B) into pin 26 of the socket adjacent to the IF - DEMODULATOR board. This pin is the input to the SERIAL-TO-PARALLEL converter board.

3. Synchronize the oscilloscope to the RF envelope of the transmitter signal. A convenient point to obtain this signal is on R_n of the IF - AMPLIFIER BOARD.

4. With proper synchronization, the demodulated code pattern of the transmitter should be visible at the beginning of the scope trace. Channel noise should be observed between code patterns. The duration of the code pattern should be 22 milliseconds minimum, with a peak-to-peak amplitude of 10 volts $\pm$ 5%.

5. If the pattern is not observable, replace the IF - DEMODULATOR BOARD.

5.7.3.2.3 SERIAL-TO-PARALLEL CONVERTER BOARD

The serial-to-parallel converter board may be simply checked for faults if the boards ahead of it in the receiver system are functioning properly, and a transmitter unit is available to generate a valid encoded signal to which the S/P circuitry was designed to respond.

The transmitter unit is activated to transmit a continuous series of code patterns. The oscilloscope is synchronized to the strobe signal on pin 29 of any of the decoder board sockets, and the scope is utilized to look at each data line to the decoder board socket pins 9, 10, 11, 12, 13, 14, 15, and 30. These are, respectively, data lines A_0 through A_7.

The S/P board function may be checked by the following steps:

1. Insert S/P converter board into PDS receiver card cage along with an RF Amplifier and an IF Demodulator board that are known to be in working order. The three Channel Decoder boards are removed for this test.

2. Activate the PDS transmitter unit by removing the covert switch shorting cap.

3. Determine if a strobe signal is present at pin 29 of any one of the three Channel Decoder board sockets. A strobe pulse should be present for each transmitter pulse. The repetition rate of the pulses should be 2.44 HZ, and the pulse width, 100 microseconds. If the pulses are not present, the S/P Converter board is faulty.

4. If strobe pulses are present, synchronize one display channel of the oscilloscope to the pulses to obtain a display.

5. Utilize a second channel on the oscilloscope to determine the logic states of the data lines A_0 through A_7 during the time the strobe signal is at a logic "1" level. The data, which are on pins 9, 10, 11, 12, 13, 14, 15, and 30 (A_0 - A_7), should be in the states corresponding to the "one-zero" pattern, established by the encoding

switch in the PDS transmitter unit, when the strobe signal is in a "one" state. If this condition is not obtained, the S/P Converter board is faulty.

6. Check pin 28 of any of the Channel Decoder board sockets for STR (short-term reset) pulses. They should occur at slightly longer than one second intervals and have a duration of 30 microseconds minimum. An absent pulse means a faulty board.

7. Check pin 26 of any Channel Decoder board socket for LTR (long-term reset) pulses. They should occur at approximately 6.5 second intervals and have a duration of approximately 100 microseconds. If the pulses are absent, the board is faulty.

8. Check channel alarm mono-stable multivibrator circuit by measuring the output on resistor R5 of the motherboard when pin 18 or pin 20 of either Channel Decoder board socket is forced to a logic "one" state by jumping it to +10 volts. The voltage on the end of R5 next to the barrier strip should reach a logic "one" level and reset to a logic "0" state after approximately 10 seconds. A fault is indicated if this condition is not achieved.

9. Check the tamper alarm multivibrator circuit by monitoring pin 1 of integrated circuit U1 on the mother board. The pin should reach a logic "one" state for at least 1.6 seconds after the antenna is disconnected from the receiver unit, or the tamper switch is actuated momentarily. If the antenna circuit remains disconnected or the tamper switch remains low, failure to achieve this condition indicates a fault on the S/P Converter board.

5.7.3.2.4 CHANNEL DECODER BOARD

The PDS receiver system contains three Channel Decoder boards. This redundancy allows some fault conditions to be isolated to a particular decoder board with relative ease. For test purposes, all six receiver channels (two per Channel Decoder board) may be set to decode the same transmitted code. A faulty channel will fail to provide an indication on the Channel Alarm LED.

For fault conditions where a data line is shorted to a "one" or "zero" state by a bad IC component, and that state does not correspond to the transmitted code pattern, none of the six channels will provide an alarm indication. To preclude this situation, the Channel Decoder boards should be checked singularly, and the transmitted code pattern varied. A set of code patterns to check all DIP switch positions would include all "ones", all "zeros", and alternating "ones" and zeros".

A channel alarm indication should cause the voltage on resistor R5 of the mother board to set to a logic "one" level. The voltage will remain at this level even through the Channel Alarm indicator is cycling on and off. The level should remain at a logic "one" level for approximately 10 seconds after the last Channel Alarm indication. The voltage on R should be measured at the end of the resistor closest to the barrier strip.

5.8 ALIGNMENT AND ADJUSTMENT

5.8.1 TRANSMITTER RF ALIGNMENT PROCEDURE

The following test equipment and alignment tools, or their equivalents, are required for the alignment of the various stages of the PDS transmitter unit:

1) Tektronix Model 7L13 Plug-in Spectrum Analyzer.
2) Tektronix Model 7603 Oscilloscope (mainframe).
3) Tektronix 7633 oscilloscope with 7A26 and 7B53A plug-in modules.
4) Johansen tuning tool, Model 4093.
5) GC (Div of Electrocraft) tuning tool, Model GC5066.
6) Hewlett - Packard, Model HP5328A frequency counter.
7) Textronix Model P6062B Oscilloscope Probe.

5.8.1.1 SPECIAL FIXTURES AND EQUIPMENT

1) Modified PDS Transmitter Housing with access holes for tuning
2) Four(4) foot RG58/u coax cable with BNC connector and 1/4" diameter pick-up loop.
3) PDS receiver antenna with 6 feet, or more, of coax cable with appropriate connectors (Type "N") for mating with Spectrum Analyzer or receive unit.
4) PDS receiver unit with appropriate power supply (20 Volt, 0.1 amp., DC).

5.8.1.2 INITIAL ALIGNMENT PROCEDURE

1. Connect 9V battery to transmitter battery terminals (Two NEDA Type 1307A 4.5 Volt, Alkaline). Make sure that the jumper between the two batteries is connected.

2. Remove covert switch shorting plug from input connector. The digital circuitry should become active approximately 4.5 seconds after the jumper has been removed.

3. Connect oscilloscope probe (Tektronix Model P6062B) to the frequency counter input. Connect probe ground clip to the center conductor pin of the covert switch input connector. Clip probe to the end of resistor R_7 nearest the clock oscillator coil L_1. Set counter to obtain a frequency reading. Adjust coil L_1 to obtain an 80 KHz $\pm$ clock oscillator frequency. Remove oscilloscope probe from the transmitter to continue alignment.

4. Connect the coax cable with 1/4" diameter pick-up loop to Spectrum Analyzer input. Tune spectrum analyzer center frequency to the Transmitter oscillator frequency (68.75 MHZ). Place pick-up loop near oscillator inductor L_2. A pulsing signal should be indicated on the spectrum analyzer. If not, adjust oscillator trimmer cap. C_{11} to obtain signal at correct frequency. The oscillator should be in operation when the capacitor plates are approximately 80% meshed.

5. Return the Spectrum Analyzer to twice the oscillator frequency. Place the pick-up loop of the coax cable connected to the analyzer input between the two turns of the first doubler coil L_3 closest to the coupling coil L_4. A pulsing output, twice the oscillator frequency

(137.5 MHZ), should be observed on the Spectrum Analyzer screen. Adjust trim cap. C_{15} to obtain a peak pulse level in excess of OdBM.

6. Retune Spectrum Analyzer to the final output frequency (275 HMZ).

7. Place cable pick-up loop above second doubler coil L_6. The pick-up loop should be oriented to the same plane as that of L_6 and placed within 1/16" of L_6.

   Adjust trim caps. C_{17} and C_{18} until the power coupled into the spectrum analyzer exceeds OdBM. Obtain a peak reading. If a OdBM level cannot be achieved, increase coupling between inductors L_3 and L_4 by pushing coil L_4 closer to coil L_3. The spacing between the two coils can vary between 1/4 inch and 1/16 inch. The coupling should be adjusted, and the tuning of C_{17} and C_{18} continued until a peak reading of OdBM minimum and +3dBM maximum is obtained.

5.8.1.3 FINAL ALIGNMENT

The final alignment of the transmitter unit cannot be achieved until the transmitter PCB, with all switches and batteries connected, is mounted into the plastic housing.

The PCB is mounted to the housing cover with the six #2-56 screws in the normal manner. The cover, with sealing gasket in place, is utilized along with a special rear housing, containing adjustment clearance holes, to enable final transmitter alignment.

1. Connect Receiving Antenna to Spectrum Analyzer input with appropriate coaxial cable.

2. Remove Shorting Plug from covert switch input.

3. Tune Spectrum Analyzer to the transmitter frequency (275 MHZ). Set the analyzer bandwidth to 30 KHZ, the resolution to 50 KHZ/DIV., and a full-scale sensitivity of 0dBM.

4. Holding the transmitter unit within a few feet of the Receiving Antenna, observe the pulsing output spectrum of the transmitter unit.

5. With the transmitter unit held at a fixed distance from the receiving antenna attached to the spectrum analyzer, adjust trim cap. C_{24} to obtain a peak reading on the spectrum analyzer. This adjustment should have a relatively broad range.

6. Adjust trim caps. C_{11}, C_{15}, C_{17}, and C_{18}, consecutively, to achieve the highest peak reading on the spectrum analyzer.

7. Readjust cap C_{24} for highest transmitter output.

8. Set spectrum analyzer sensitivity to obtain +20dBm full scale.

9. Stand transmitter unit on Receiving Antenna ground plane approximately 1" (one inch) from the antenna rod.

10. Tilt the transmitter unit against the antenna rod.

11. The peak reading of the spectrum analyzer should be between +10dBm and +13dBm. If the output is greater than +13dBm, reduce coupling of inductor L_7 by slightly decreasing its area. If the transmitter output is still too high, reduce coupling of inductor L_4 to L_3 by increasing spacing between the coils. Readjust all trim caps. to

achieve final peaking after any coupling adjustment.

12. If the transmitter output is less than +10dBm, repeat the procedures in step 11, but increase coupling by moving L_3 closer to L_4.

13. When steps 1 through 12 have been completed, the rf envelope of the transmitter should be observed through a PDS receiver IF in order to ensure that an on-channel, undistorted waveform is achieved.

The transmitter RF envelope may be observed with an oscilloscope connected to R_3 of the Receiver IF Demodulator PCB.

The RF envelope should be a minimum of 23 milliseconds in length and when the scope sweep speed is increased to 100 to 300 microseconds/division symmetrical AM modulated rf envelope, indicating a minimum of 70% modulation should be observed. If not, adjust transmitter oscillator trimmer C_{11} until the observed envelope has the characteristics described. If the oscillator trim cap. is adjusted, readjustment of the other capacitors in the transmitter amplifier may have to be done to achieve the transmitter output power indicated in step 12.

5.8.2 RECEIVER ALIGNMENT PROCEDURE

5.8.2.1 RF BOARD

Equipment Required

HP8640B	1) RF generator 265 to 285 MHZ tuning range.
Tektronix 7633 Main Frame 7A26 dual Trace AMP, 7B53A a dual time base	2) HIGH Frequency oscilloscope BW approx. 100 MHZ, Sensitivity smv/cm
Fluke	3) DVM - 3 digit min.
LAMBDA	4) Power supply 0-20V min, 150 ma. D.C.
HP5328A	5) Frequency Counter

1. Connect power supply to terminals 7 and 8 of the barrier strip on the mother board. Terminal seven(7) is positive and terminal eight(8) is negative. With no boards plugged into the mother board, the current drawn from the power supply should be less than 5 ma., with a power supply setting of 20 volts output.

2. Plug in the RF board into channel nearest the tamper switch. The load current should be less than 25 ma. with a proper functioning RF board.

3. With low capacity scope probe TEK. P6062B (15pf max.) measure local oscillator #1 output voltage at junction of R22 and R23. The level should be 1.2 VP-P minimum.

4. Transfer probe to frequency of counter input. The frequency should be adjusted with the trim cap. C27 to obtain a frequency equal to

difference between the desired and measured frequencies. For example, if the desired channel frequency is 275MHZ, then the first local oscillator frequency is (257 MHZ - 60 MHZ) ÷ 3 = 71.667 MHZ.

5. With low capacity scope probe (15 pf max.) measure local oscillator #2 output voltage at the junction of R27 and the source of FET Q7. The level should be 2.0 VP-P minimum.

6. Transfer probe to frequency counter. If frequency is not equal to this value, adjust the trim cap. C38 to obtain the correct value.

7. Remove trip from TEK.P6062B Scope probe. Place probe multiplier switch in X10 position. Insert tip of probe into pin 26 of the socket in mother board adjacent to the RF board.

8. Connect RF signal generator to receive antenna input terminal. Set generator frequency to 275 MHZ and output level to - 20 dbm (approx 22 mv). Set AM modulator of signal generator to 50% at 1 KHZ.

9. Increase oscilloscope gain until a modulated RF envelope appears on screen. Adjust the tuning coves in the three 60 MHZ IF amplifier inductors (L_4, L_5, L_6) to maximize the output signal at pin 26 of the mother board connector.

10. Adjust trim caps. C_1, C_4, C_8, and C_{33} to maximize output signal. As all adjustments are tuned to maximize signal output, reduce signal generator output, turn off signal generator modulation. Set signal generator output level to 500 microvolts. The peak-to-peak output voltage of the RF amplifier board should be 3 volts. If not, adjust gain control pot. R_{11} to obtain proper output.

5.8.2.2 IF DEMODULATOR BOARD

Equipment Required

HP8640B RF signal generator 10.7 MHZ tuning range

Special equipment: 3 foot coax cable (R658/u) with chip lead soldered to braid and 910 ohm resistor.

1. Complete step one of section 5.8.2.1.

2. Set RF generator output to 200 microvolts.

3. Connect coax cable with a 910 ohm resistor between ground reference and pin 11 of the RF amplifier board connector.

4. Plug IF-Demodulator board into proper connector on mother board. The current from the power supply should not exceed 22 ma.

5. Modulate RF generator 100% with 9KHZ signal.

6. Connect oscilloscope probe to output of U3 (pin 6) at junction of R13 and observe 9KHZ signal. The signal has a large noise component at a 200 microvolt RF input level.

7. Adjust inductor L3 to obtain a maximum 9 KHZ component. The adjustment is a very broad range.

8. Connect voltmeter between ground and junction of arm of pot R15 and resistor R24. Adjust pot, to obtain a voltage reading of 3.6 volts.

9. Adjust pots, R15 and R17 fully counter-clockwise.

10. Modulate Rf generator 100% with an 8.3 KHz signal.

11. Connect oscilloscope to output of demodulator board (pin 3, 18).

12. Adjust pot. R17 clockwise until the output of the IF - demodulator circuit as measured at pin 3, 18 just limits at 10 volts DC.

13. Set modulation frequency of the RF signal generator to 9 KHz.

14. Adjust pot. R15 clockwise until the DC reading of the oscilloscope is 5 volts.

SECTION 6

REPLACEABLE PARTS LIST

6.1 INTRODUCTION

This section of the manual is an illustrated parts list breakdown itemizing all assemblies and their components. Illustrations for each listing aid in locating the assemblies and components.

6.2 PARTS LIST COLUMN DESIGNATIONS

6.2.1 The REF NO. COLUMN indexes the item description to the associated illustration. In general the reference designations are listed under each assembly in alpha-numeric order.

6.2.2 The PART NO. COLUMN provides a part designation number or alpha-numeric identification for each part.

6.2.3 The DESCRIPTION COLUMN describes the salient characteristics of the component.

6.2.4 The QTY COLUMN lists the total quantity of items used in that particular assembly.

PORTABLE DURESS SENSOR
(001D00003)

REF NO.	PART NO.	DESCRIPTION	QTY
1	003D00040	Receiver, Portable Duress Assy	1
1	003D00056	Antenna, Portable Duress Assy	1
1	003D00057	Transmitter, Portable Duress Assy	1

RECEIVER ENCLOSURE SUB-ASSEMBLY
(004D00019)

REF NO.	PART NO.	DESCRIPTION	QTY
1	005D00086	Case, Portable Duress	1
2	MS35822-10D	Hinge	1
3	S-832-2	Nut, Clinch	2

RECEIVER MOTHER BOARD
(003D0034)

REF NO.	PART NO.	DESCRIPTION	QTY
1	009D00026	Board, Printed Wiring	1
2	14410	Terminal, Barrier	1
3	1N4001	Diode, Semiconductor	1
4	JAN1N4148	Diode, Semiconductor	2
5	JAN2N2222A	Transistor, Semiconductor	2
6	CKR06BX105KM	Capacitor, Fixed, Ceramic Dleclectric	1
7	CKR06BX334KM	Capacitor, Fixed, Ceramic Dielectric	1
8	LM117K	Microcircuit, Linear	1
9	RCR07G203JS	Resistor, Fixed, Carbon Composition	2
10	RCR07G272JS	Resistor, Fixed, Carbon Composition	2
11	RCR07G301JS	Resistor, Fixed, Carbon Composition	2
12	M38510/05204BCA	Microcircuit, Digital	1
13	M55302/58-B30X	Connector	6
14	NAS620-6	Washer, Flat	4
15	NAS620-4	Washer, Flat	12
16	MS35338-135	Washer, Locking, Helical Spring	12
17	MS35338-136	Washer, Locking, Helical Spring	4
18	MS35431-3	Terminal, Lug, Solder	1
19	MS35649-264	Nut, Hex	4
20	MS51957-17	Screw, Cross Recessed, Pan Head	12
21	MS51957-28	Screw, Cross Recessed, Pan Head	2
22	MS51957-30	Screw, Cross Recessed, Pan Head	2
23	748-1	Nut, Hex	12
24	RNC55H4871FM	Resistor, Fixed, Film	1
25	RNC55H6980FM	Resistor, Fixed, Film	1
26	MS25036-144	Terminal, Ring, Crimp	2
27	Type B-24, CLR 444	Wire, Stranded, 24 AWG, Yellow	7"
28	Type B-24, CLR 000	Wire, Stranded, 24 AWG, Black	6
29	214-120	Pad, Transistor	2
30	RCR07G104-JS	Resistor, Fixed, Carbon Composition	1
31	50-051-000	Connector, Sub-Miniature	1
32	SN60WRAP	Solder, Tin Lead, Alloy	A/R

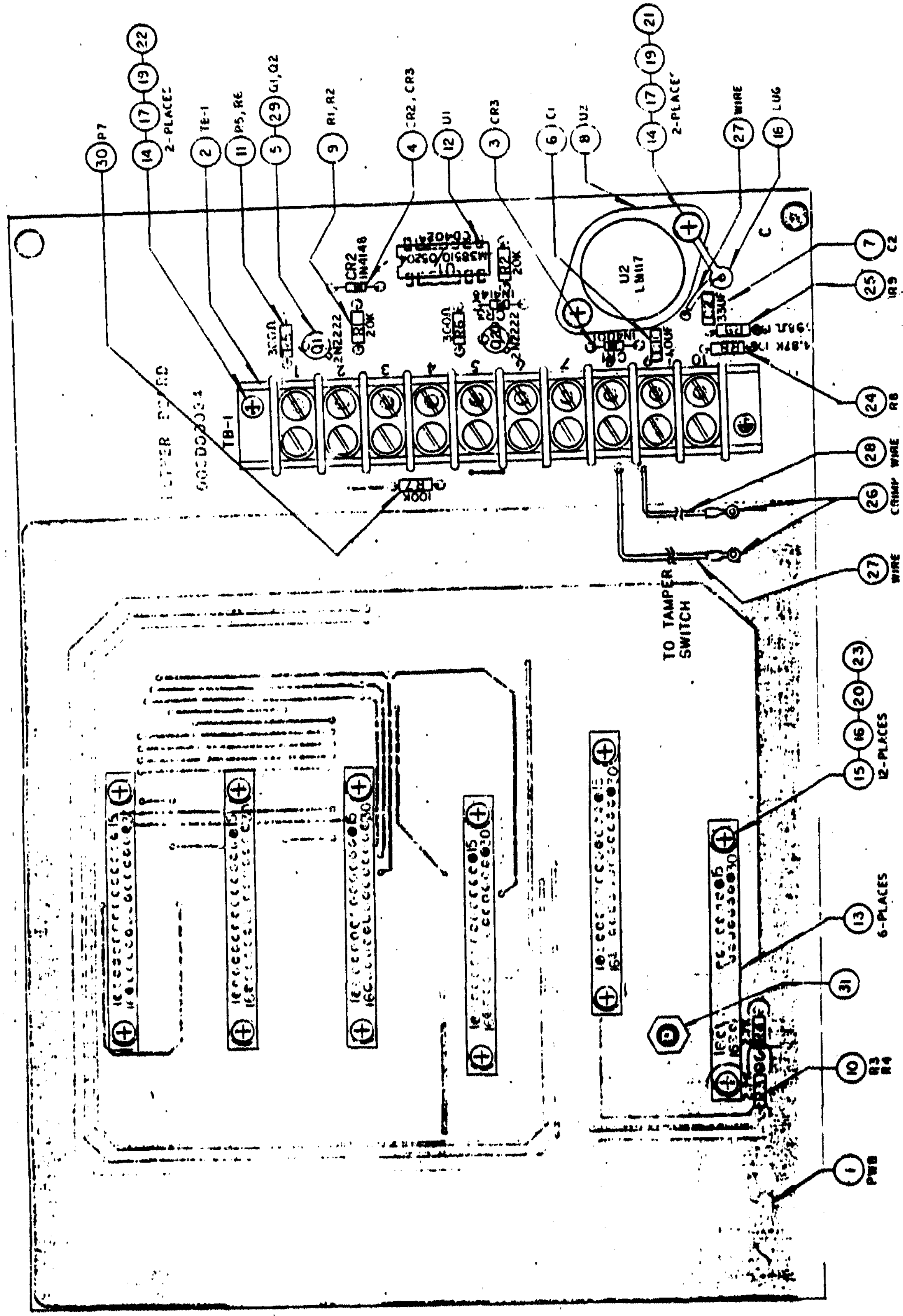

Figure 6-1. Receiver Mother Board Assembly

RECEIVER ASSEMBLY
(003C00040)

REF NO.	PART NO.	DESCRIPTION	QTY
1	003C00028	Amplifier, I.F. Assembly	1
2	003C00029	Channel Decoder Assembly	3
3	003C00030	Serial/Parallel Converter and Alarm Assembly	1
4	003C00031	Amplifier, R.F. Assembly	1
5	003D00034	Receiver Mother Board Assembly	1
6	005B00082	Plate Front	1
7	005C00083	Cover, Top	1
8	005C00084	Plate, Side, Left	1
9	005C00085	Plate, Side, Right	1
10	UG-1466/U	Connector, Sub-Miniature	1
11	RG-188/U	Cable, Coaxial	6"
12	MS35338-135	Washer, Locking, Helical Spring	24
13	MS35338-136	Washer, Locking, Helical Spring	13
14	MS51957-13	Screw, Cross Recessed Pan Ahead	24
15	MS51957-30	Screw, Cross Recessed Pan Head	4
16	MS51957-27	Screw, Cross Recessed Pan Head	6
17	MS15795-804	Washer, Flat	20
18	MS15795-806	Washer, Flat	10
19	UG58/U	Connector, R.F., Type N	1
20	MS16106-1	Switch, Snap Action	1
23	005B00093	Plate, Rear	1
24	9794-A-0632-17	Standoff	1
25	004D00019	Subassembly, Enclosure	1
26	MS16995-25	Screw, Cap Socket HD S.S. 8-32,3/8	2

RECEIVER I.F. AMPLIFIER
(003C00028)

REF NO.	PART NO.	DESCRIPTION	QTY
1	009B00022	Board, Printed Wiring	1
2	1N4148	Diode, Semiconductor	6
3	JAN2N2857	Transistor, Semiconductors	1
4	100113	Coil, Radio Frequency	1
5	100126	Coil, Radio Frequency	1
6	900-372-25	Filter, Bandpass, Crystal	1
7	CA3160BS	Microcircuit, Linear	2
8	CCR07CG333JK	Capacitor, Fixed, Ceramic Dielectric	1
9	CD4046BD	Microcircuit, Linear	1
10	CKR05BX103KM	Capacitor, Fixed, Ceramic Dielectric	7
11	CKR05BX222KM	Capacitor, Fixed, Ceramic Dielectric	2
12	CKR06BX334KM	Capacitor, Fixed, Ceramic Dielectric	1
13	CKR05BX471KM	Capacitor, Fixed, Ceramic Dielectric	2
14	CMR06F102JPDM	Capacitor, Fixed, MICA Dielectric	1
15	CMR05E360JPDM	Capacitor, Fixed, MICA Dielectric	1
16	HSCH-3486	Diode, Semiconductor, Hot Carrier	1
17	RCR07G101JS	Resistor, Fixed, Carbon Composition	1
18	RCR07G103JS	Resistor, Fixed, Carbon Composition	1
19	RCR07G104JS	Resistor, Fixed, Carbon Composition	4
20	RCR07G152JS	Resistor, Fixed, Carbon Composition	1
21	RCR07G2473JS	Resistor, Fixed, Carbon Composition	1
22	RCR07G273JS	Resistor, Fixed, Carbon Composition	1
23	RCR07G303JS	Resistor, Fixed, Carbon Composition	1
24	RCR07G334JS	Resistor, Fixed, Carbon Composition	1
25	RCR07G335JS	Resistor, Fixed, Carbon Composition	1
26	RCR07G512JS	Resistor, Fixed, Carbon Composition	2
27	RCR07G682JS	Resistor, Fixed, Carbon Composition	1
28	RJR24CX502M	Resistor, Variable	1
29	RJR24CX104M	Resistor, Variable	2
30	SNC55H3651FM	Resistor, Fixed, Film	6
31	RNC55H2493FM	Resistor, Fixed, Film	5
32	MS21402-25	Coil, Radio Frequency	1
33	LM741	Microcircuit, Linear	2
34	M55302/57-A30X	Connector	1
35	MS51957-15	Screw, Cross Recessed Pan Head	2
36	MS35338-135	Washer, Locking, Helical Spring	4
37	NA620-4	Washer, Flat	4
38	748-1	Nut, Hex, Series WTBRP	2
39	MS35649-244	Nut, Hex	2
40	214-120	Pad, Transistor	1
41	32559	Pad, Microcircuit	4
42	M39014/01/1317	Capacitor Fixed Ceramic Dielectric	1

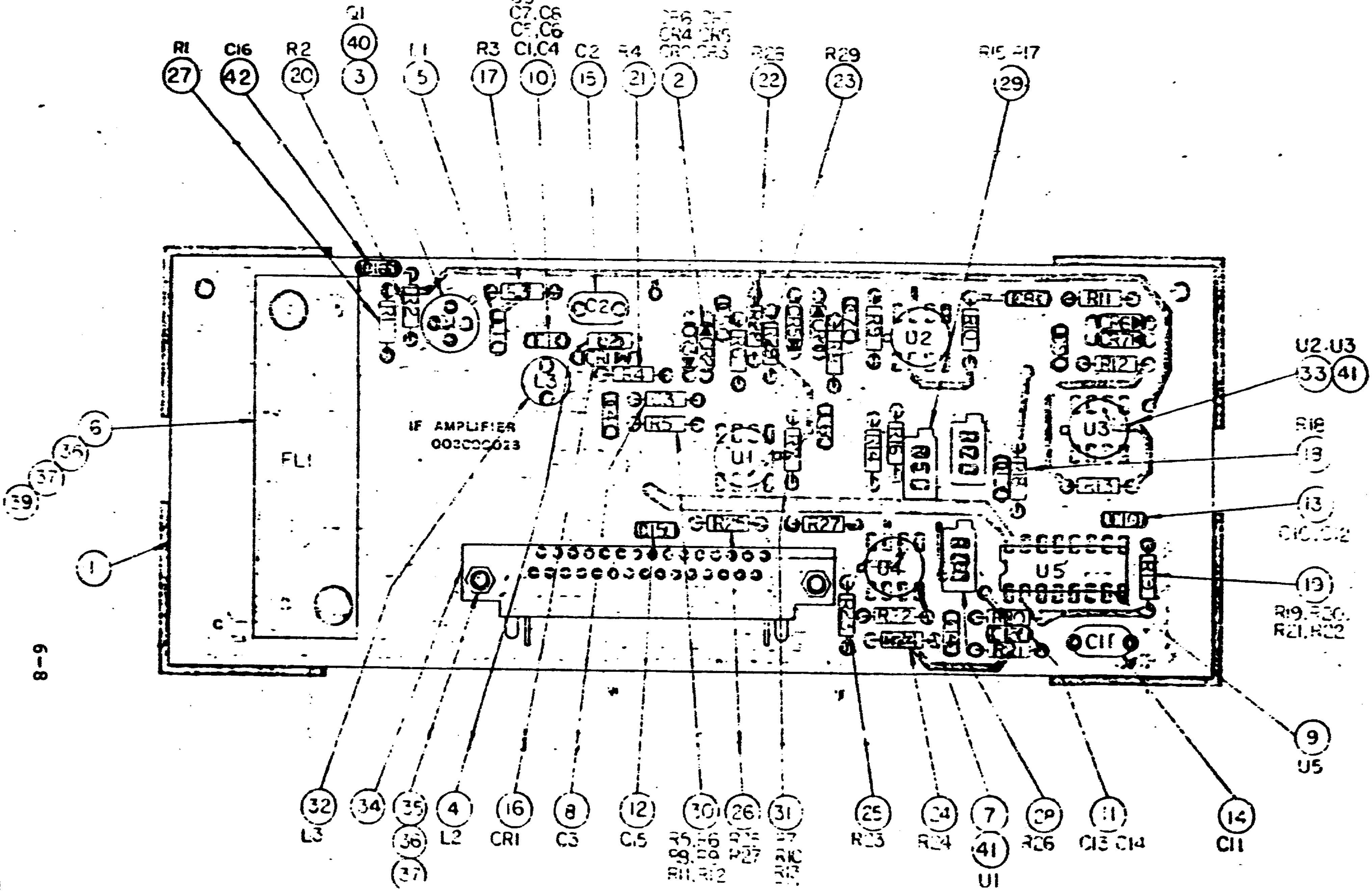

Figure 6-2. Receiver IF Amplifier
Circuit Assembly

CHANNEL DECODER
(003C00029)

NO.	NO.	DESCRIPTION	QTY
1	009C00020	Board, Printed Wiring	1
2	76PSB08	Switch, Rocker	2
3	550-2405	Diode, Semiconductor, Light Emitting	3
4	CD4520BD	Microcircuit, Digital	1
5	CD4585BD	Microcircuit, Digital	4
6	CKR05BX102KM	Capacitor, Fixed, Ceramic Dielectric	2
7	CKR06BX334KM	Capacitor, Fixed, Ceramic Dielectric	1
8	RCR07G104JS	Resistor, Fixed, Carbon Composition	2
9	RCR07G204JS	Resistor, Fixed, Carbon Composition	16
10	RCR07G222JS	Resistor, Fixed, Carbon Composition	2
11	4011	Microcircuit, Digital, Nand Gate	3
12	4001	Microcircuit, Digital, Nor Gate	1
13	M55302/57-A30X	Connector	1
14	MS51957-15	Screw, Cross Recessed Pan Head	2
15	MS35338-135	Washer, Locking, Helical Spring	2
16	NAS620-4	Washer, Flat	2
17	748-1	Nut, Hex, Series WTBPR	2
18	JAN1N4148	Diode, Semiconductor	2

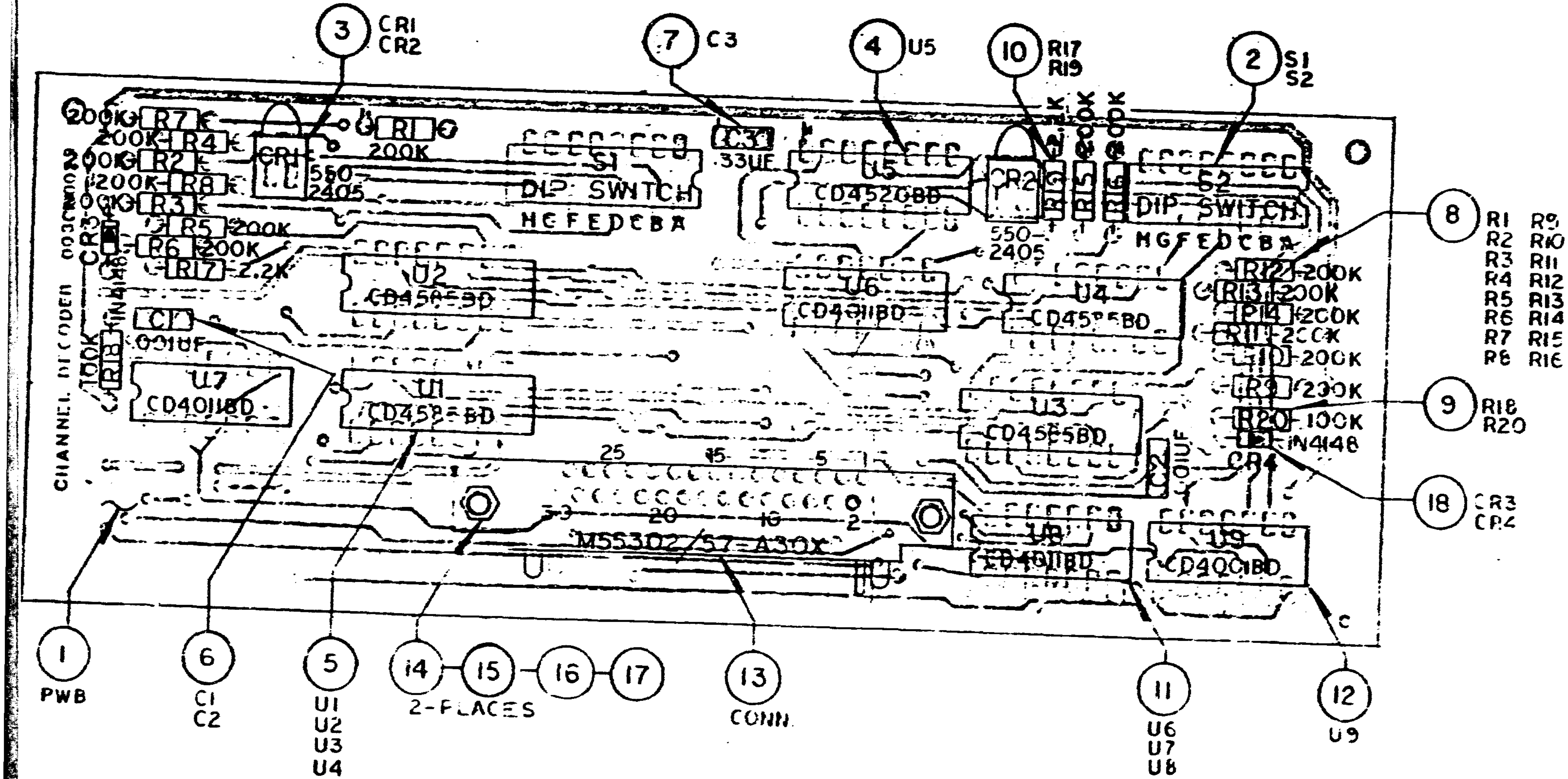

Figure 6-3. Channel Decoder Circuit Assembly

SERIAL/PARALLEL CONVERTER
(003C00030)

REF NO.	PART NO.	DESCRIPTION	QTY
1	009C00023	Board, Printed Wiring	1
2	JAN2N2222A	Transistor, Semiconductor	1
3	CCR05CG222JM	Capacitor, Fixed Ceramic Dielectric	1
4	CCR06CG512JM	Capacitor, Fixed Ceramic Dielectric	1
5	CCR05CG471JM	Capacitor, Fixed Ceramic Dielectric	1
6	4078	Microcircuit, Digital 8 Input Nor Gate	1
7	4520	Microcircuit, Digital, Dual Up Counter	2
8	4538	Microcircuit, Digital Dual Monostable MV	2
9	CKR05BX102KM	Capacitor, Fixed, Ceramic Dielectric	5
10	CKR05BX103KM	Capacitor, Fixed, Ceramic Dielectric	1
11	CKR06BX105KM	Capacitor, Fixed, Ceramic Dielectric	1
12	CKR06BX334KM	Capacitor, Fixed, Ceramic Dielectric	2
13	RCR07G103JS	Resistor, Fixed, Carbon Composition	1
14	RCR07G104JS	Resistor, Fixed, Carbon Composition	11
15	RCR07G106JS	Resistor, Fixed, Carbon Composition	1
16	RCR07G332JS	Resistor, Fixed, Carbon Composition	1
17	RCR07G515JS	Resistor, Fixed, Carbon Composition	1
18	RNR55C8253FM	Resistor, Fixed, Film	1
19	4023	Microcircuit, Digital, Triple 3-Input Nand Gate	1
20	4001	Microcircuit, Digital, Nor Gate	1
21	4017	Microcircuit, Digital, Decade Counter/ Divider	1
22	4040	Microcircuit, Digital, 12 Bit Binary Counter	1
23	4015	Microcircuit, Digital	2
24	M55302/55-430X	Connector	1
25		Coil, Radio Frequency	1
26	MS51957-15	Screw, Cross Recessed Pan Head	2
27	MS35338-135	Washer, Locking, Helical Spring	2
28	NAS620-6	Washer, Flat	2
29	748-1	Nut, Hex, Series WTBPR	2
30	314-120	Pad, Transistor	1
31	RCR07G473JS	Resistor, Fixed Carbon Composition	1
32	RCR07G103JS	Resistor, Fixed Carbon Composition	1
33	RCR07G334JS	Resistor, Fixed Carbon Composition	1

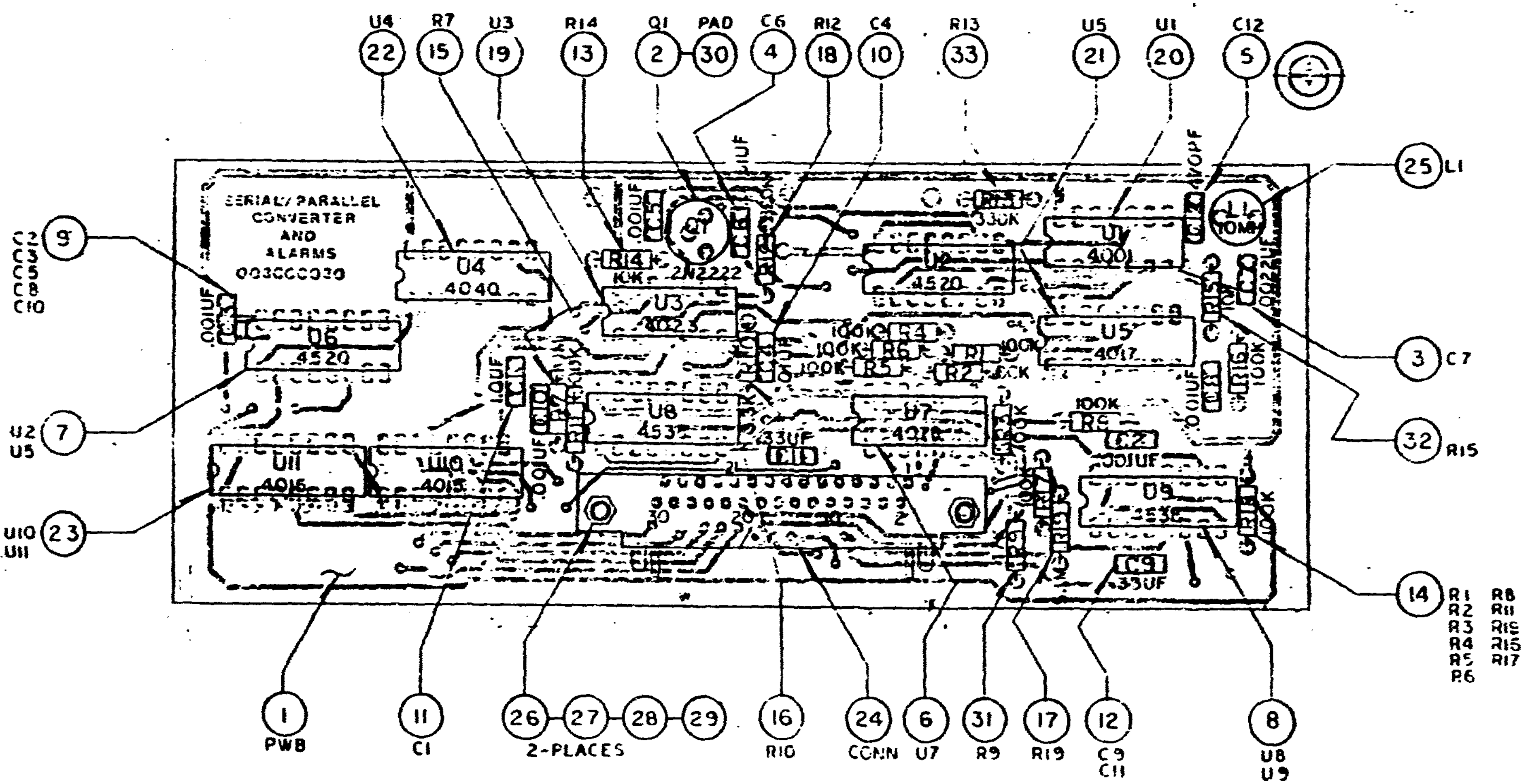

Figure 6-4. Serial/Parallel Converter & Alarm Circuit Assy.

RECEIVER R.F. AMPLIFIER
(003C00031)

REF NO.	PART NO.	DESCRIPTION	QTY
1	009C00021	Board, Printed Wiring	1
2	6380-4	Coil, Variable, Radio Frequency	3
3	9615	Capacitor, Variable, Ceramic Dielectric	4
4	100071	Coil, Fixed, Radio Frequency	2
5	100076	Coil, Fixed, Radio Frequency	1
6	100088	Coil, Fixed, Radio Frequency	1
7	100090	Coil, Fixed, Radio Frequency	1
8	100113	Coil, Fixed, Radio Frequency	1
9	189-0503-005	Capacitor, Variable, Air Dielectric	2
10	CKR05BX102KM	Capacitor, Fixed, Ceramic Dielectric	6
11			
12	CMR03C1R0D0CM	Capacitor, Fixed, MICA Dielectric	1
13	CMR03C2R0D0CM	Capacitor, Fixed, MICA Dielectric	3
14			
15			
16	CMR03E220D0CM	Capacitor, Fixed, MICA Dielectric	4
17	CMR03F221J0YM	Capacitor, Fixed, MICA Dielectric	5
18	CMR03F331J0YM	Capacitor, Fixed, MICA Dielectric	1
19	CMR03E390J0YM	Capacitor, Fixed, MICA Dielectric	2
20		Capacitor, Fixed, MICA Dielectric	
21	CMR03F401J0YM	Capacitor, Fixed, MICA Dielectric	4
22			
23	CMR03E750J0YM	Capacitor, Fixed, MICA Dielectric	3
24	CR-56A/U	Crystal Unit, Quartz 68,333MHZ to 75,000 MHZ	1
25	CR-67A/U	Crystal Unit, Quartz, 49,3000MHZ	1
26	JAN2N2857	Transistor, Semiconductor	1
27	JAN2N4416A	Transistor, Semiconductor, Field Effect	2
28	3N200	Transistor, Semiconductor, Field Effect	4
29	RCR07G101JS	Resistor, Fixed, Carbon Composition	9
30	RCR007G102JS	Resistor, Fixed, Carbon Composition	2
31	RCR07G103JS	Resistor, Fixed, Carbon Composition	5
32	RCR07G104JS	Resistor, Fixed, Carbon Composition	1
32A	100-095	Pad, Transistor	7
33	RCR07G221JS	Resistor, Fixed, Carbon Composition	1
34	RCR07G151JS	Resistor, Fixed, Carbon Composition	2
35	RCR07G223JS	Resistor, Fixed, Carbon Composition	1
36	RCR07G224JS	Resistor, Fixed, Carbon Composition	3
37	SCR07G435JS	Resistor, Fixed, Carbon Composition	1
38	RCR07G473JS	Resistor, Fixed, Carbon Composition	1
39	RCR07G825JS	Resistor, Fixed, Carbon Composition	1
40	RJR24CW503M	Resistor, Variable	1
41	M55302/57-A30X	Connector	1
42	MS51957-15	Screw, Cross Recessed Pan Head	2
43	MS35338-135	Washer, Locking, Helical Spring	2
44	NAS420-C6	Washer, Flat	2
45	748-1	Nut, Hex, Series WTBPR	2
46	100069	Coil, Fixed Radio Frequency	1
47	CMR0305R0D0CM	Capacitor, Fixed, MICA Dielectric	1
48	CMR03E270D0CM	Capacitor, Fixed, MICA Dielectric	1
49	CMR03E680J0YM	Capacitor, Fixed, MICA Dielectric	1

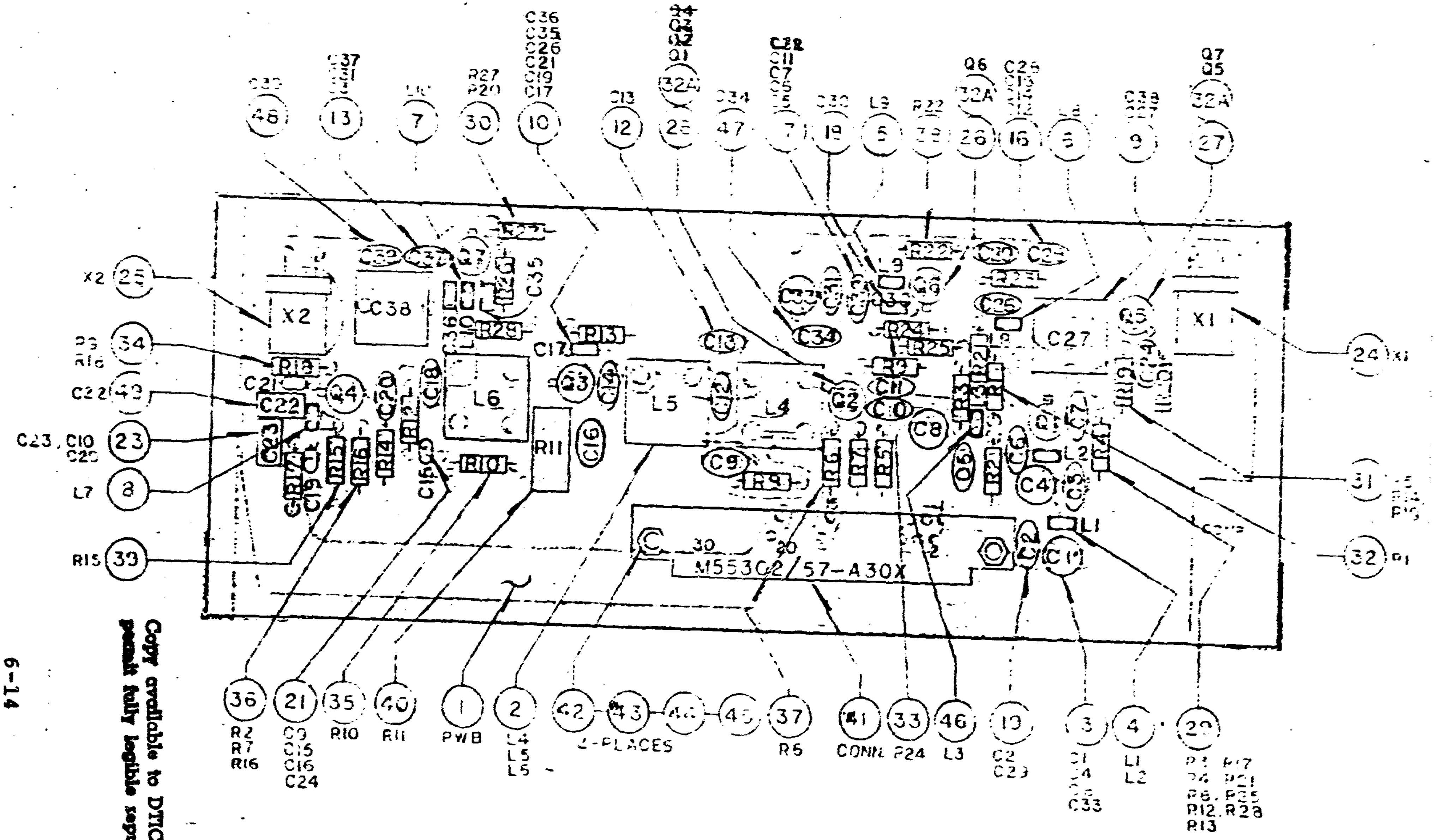

Figure 6-5. Receiver RF Amplifier Circuit Assembly

ANTENNA RECEIVING ASSEMBLY
(003D00056)

REF NO.	PART NO.	DESCRIPTION	QTY
1	005D00142	Base, Antenna	1
2	005C00143	Cover, Base	1
3	005C00144	Plate, Mtg., Base	1
4	005C00145	Bracket, Mounting	1
5	005B00146	Block, Mounting, Antenna	1
6	005C00174	Antenna	1
7	030C00063	Support, Antenna (Teflon)	1
8	AN960C1216L	Washer, Flat	1
9	NAS620C4	Washer, Flat	4
10	NAS620C6	Washer, Flat	8
11	NAS620C10	Washer, Flat	3
12	NAS620C416	Washer, Flat	1
13	UG58/U	Connector, R.F., Type N	1
14	MS35338-135	Washer, Lock-Spring	4
15	MS35338-136	Washer, Lock-Spring	8
16	MS35338-138	Washer, Lock-Spring	3
17	MS35338-139	Washer, Lock-Spring	1
18			
19	MS35649-264	Nut, Plain, Hex	6
20	MS35649-2254	Nut, Plain, Hex	1
21	MS35650-304	Nut, Plain, Hex	3
22	MS51957-5	Screw, Machine, Pan HD., Cross-Recessed	1
23	MS51957-14	Screw, Machine, Pan HD., Cross-Recessed	4
24	MS51957-28	Screw, Machine, Pan HD., Cross-Recessed	8
25	MS51957-82	Screw, Machine, Pan HD., Cross-Recessed	1
26	MS51958-64	Screw, Machine, Pan HD., Cross-Recessed	3
27	MS35691-59	Nut, Plain, Hex (jam)	1
28	SN60WRAP	Solder, Tin Lead Alloy	A/R
29		Terminal Lug, Ring Tip	1
30	030B00078	Wire, Tinned Copper, Solid (Belden #8013-100)	1
31	MS51957-31	Screw, Machine, Pan HD., Cross-Recessed	1
32	MS35338-134	Washer, Lock-Spring	1
33	MIL-S-22473	Sealing Compound	A/R

TRANSMITTER, PORTABLE DURESS SENSOR
(003B0057)

REF NO.	PART NO.	DESCRIPTION	QTY
1	003D00032	Transmitter, R.F., Digitally Encoded Assy	1
2	005D00117	Housing, Transmitter	1
3	005C00118	Cover, Housing, Transmitter	1
4	005C00119	Retainer, Belt	1
5		Gasket, Sealing	1
6	BP-1048	Boot, Rubber Sealing	2
7	50-001-0020	Cap, End, Shorting	1
8	531	Battery, Alkaline	2
9	MS51957	Screw, Machine, Pan Hd. Cross Recessed	2
10	MS51957	Screw, Machine, Pan Hd. Cross Recessed	6
11	MS51957	Screw, Machine, Pan Hd. Cross Recessed	2

RF TRANSMITTER ASSEMBLY
(PL004N0032)

REF NO.	PART NO.	DESCRIPTION	QTY
1	009C00024	Board, Printed Wiring	1
2	030B00064	Coil, Fixed, R.F.	1
3	030B00065	Coil, Fixed, R.F.	1
4	030B00066	Coil, Fixed, R.F.	1
5	030B00067	Coil, Fixed, R.F.	1
6	030B00068	Coil, Fixed, R.F.	1
7	030B00069	Coil, Fixed, R.F.	1
8	265	Clip, Battery, Male	1
9	265	Clip, Battery, Male	1
10	CR-67A/U	Crystal Unit, Quartz	1
11	CCR05CG221JM	Capacitor, Fixed, Ceramic Dielectric	1
12	CCR05CG222JM	Capacitor, Fixed, Ceramic Dielectric	1
13	CCR05CG471JM	Capacitor, Fixed, Ceramic Dielectric	1
14	CDR21BG471CKTM	Capacitor, Fixed, Chip, Ceramic Dielectric	4
15	CKR05G334KM	Capacitor, Fixed, Ceramic Dielectric	1
16	CKR05BX101KM	Capacitor, Fixed, Mica Dielectric	4
17	CKR05BX102KM	Capacitor, Fixed, Ceramic Dielectric	1
18	CKR05BX103KM	Capacitor, Fixed, Ceramic Dielectric	2
19	CKR05BX562KM	Capacitor, Fixed, Ceramic Dielectric	2
20	CMR03C5R0D0CM	Capacitor, Fixed, Mica Dielectric	1
21	CMR03C7R0D0CM	Capacitor, Fixed, Mica Dielectric	2
22	CMR03E150J0YM	Capacitor, Fixed, Mica Dielectric	1
23	CMR03E330J0YM	Capacitor, Fixed, Mica Dielectric	1
24	CMR03E750J0YM	Capacitor, Fixed, Mica Dielectric	1
25	CMR03E151JPDM	Capacitor, Fixed, Mica Dielectric	1
26	JAN1N4148	Diode, Semiconductor	2
27	JAN2N2222A	Transistor, Semiconductor	1
28	JAN2N2857	Transistor, Semiconductor	3
29	JAN2N2907A	Transistor, Semiconductor	1
30	JAN2N6604	Transistor, Semiconductor	1
31	M8805/101-003	Switch, Snap Action	1
32	4023	Microcircuit, Digital, Triple 3-Input Nand Gate	1
33	4001	Microcircuit, Digital, Nor Gate	1
34	4040	Microcircuit, Digital, 12 Bit Binary Counter	2
35	4021	Microcircuit, Digital, 8 Bit Static Shift Register	2
36	M39002/1E-5610	Capacitor, Fixed, Tantalum Dielectric	1
37	RG-402	Cable, Coaxial	
38	RCR07G100JS	Resistor, Fixed, Carbon Composition	1
39	RCR07G102JS	Resistor, Fixed, Carbon Composition	2
40			
41	RCR07G104JS	Resistor, Fixed, Carbon Composition	4
42	RCR07G105JS	Resistor, Fixed, Carbon Compositon	2
43	RCR07G106JS	Resistor, Fixed, Carbon Composition	1
44	RCR07G223JS	Resistor, Fixed, Carbon Composition	3
45	RCR07G332JS	Resistor, Fixed, Carbon Composition	1
46	RCR07G333JS	Resistor, Fixed, Carbon Composition	1

RF TRANSMITTER ASSEMBLY
(003B0032)

REF NO.	PART NO.	DESCRIPTION	QTY
47	RCR07G470JS	Resistor, Fixed, Carbon Composition	1
48	RCR07G471JS	Resistor, Fixed, Carbon Composition	1
49	RCR07G472JS	Resistor, Fixed, Carbon Composition	1
50	RCR07G561JS	Resistor, Fixed, Carbon Composition	1
51	RCR07G562JS	Resistor, Fixed, Carbon Composition	2
52	Type B-24-CLR-100	Wire, Electrical, 24 AWG (Black)	12"
53	MS21402-25	Coil, Radio Frequency	1
54	MS83504/1-008	Switch, Rocker	1
55	CD4520BD	Microcircuit, Digital	2
56	TPC13CO	Switch, Push Button, Momentary	
57	2N3550	Transistor, Semiconductor	2
58	9610	Capacitor, Variable, Ceramic Dielectric	1
59	9614	Capacitor, Variable, Ceramic Dielectric	1
60	9615	Capacitor, Variable, Ceramic Dielectric	1
61	898-3-R100K	Resistor, Fixed, Film	1
62	100080	Coil, Radio Frequency	1
63	100083	Coil, Radio Frequency	1
64	100-095	Pad, Transistor	7
65	50-043-7000	Connector, Sub-Miniature	1
66	187-0103-005	Capacitor, Variable, Air	1
67	Type B-24,CLR222	Wire, Electrical, 24 AWG (Red)	12"
68	SN70WRAP	Solder, Tin Lead, Alloy	A/R

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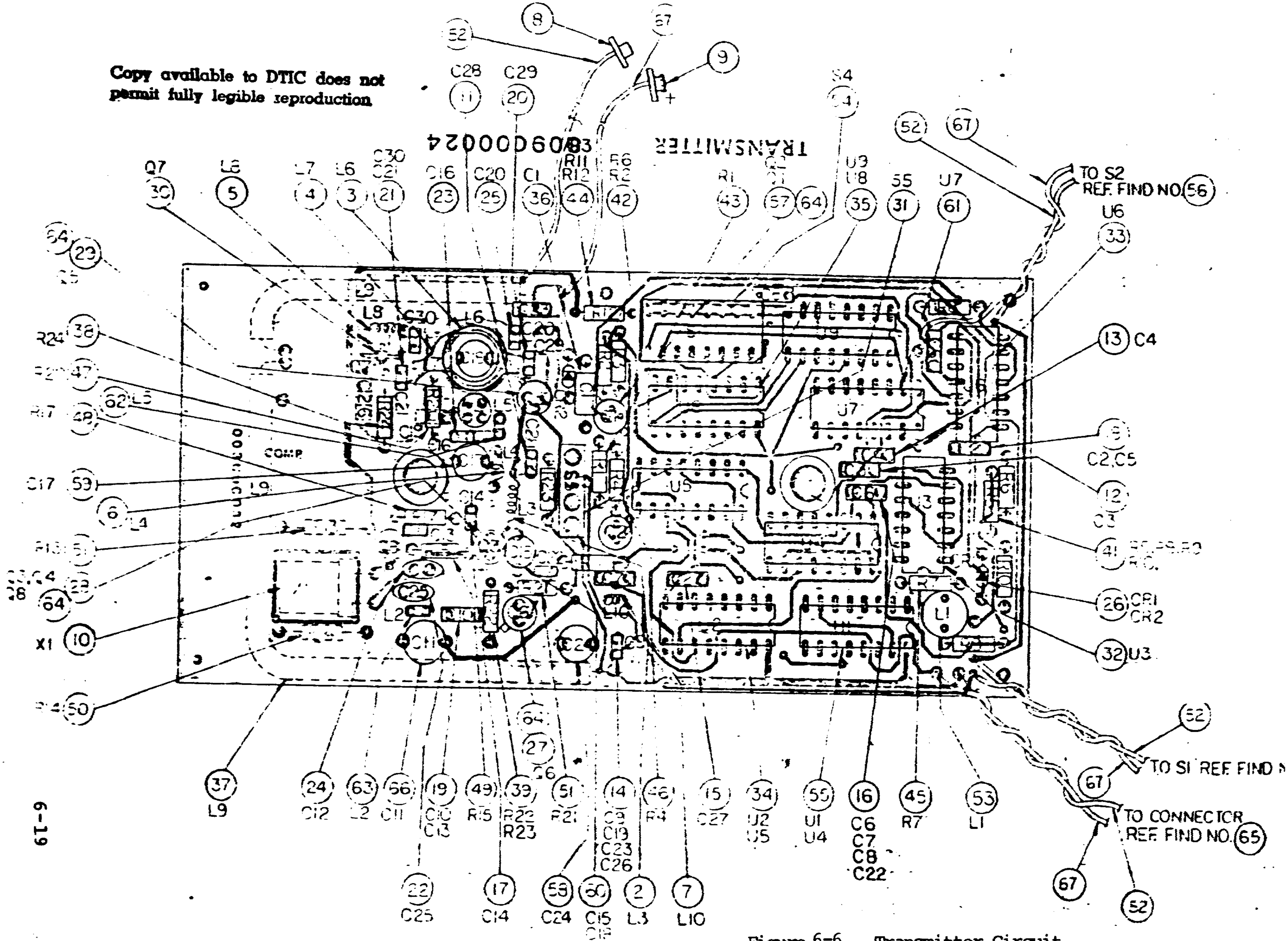

Figure 6-6. Transmitter Circuit Assembly